OKI
semiconductor

003831

MSM2758 8,192-BIT (1024 × 8) UV ERASABLE PROM
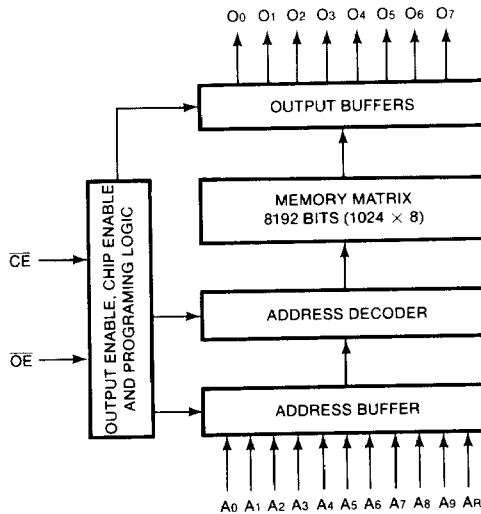
GENERAL DESCRIPTION

The Oki MSM2758 is a 8192-bit ultraviolet erasable and electrical programmable read-only memory organized as 1024-words by 8-bits using Oki's Floating Gate N-channel Silicon Gate MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Directly TTL compatible inputs, outputs and operation from a single +5V supply with low-power stand-by mode simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM2758 is offered in a 24-pin dual-in-line ceramic (AS suffix) package with quartz glass window. Operation is guaranteed from 0°C to 70°C.
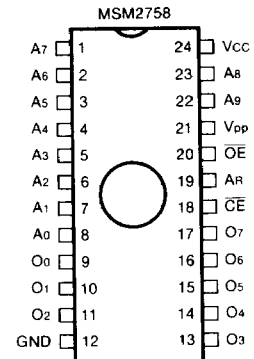
FEATURES

- 450 ns maximum Access Time
- Low Power Dissipation
  - 525 mW operating
  - 132 mW standby
- Single +5V Supply
- 1024-word × 8-bit Organization
- UV Erasable and Electrically Programmable
- Minimal Programming Time
  - 50 seconds for all 8192 bits
  - 50 milliseconds for single location
- Pin compatible with MSM2128-1, 16,384 Bit Static RAM
- Interchangeable with Intel 2758 Devices

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

MSM2758

A7	1	24 Vcc
A6	2	23 A8
A5	3	22 A9
A4	4	21 Vpp
A3	5	20 $\overline{OE}$
A2	6	19 AR
A1	7	18 $\overline{CE}$
A0	8	17 O7
O0	9	16 O6
O1	10	15 O5
O2	11	14 O4
GND	12	13 O3

A0 to A9: Address Inputs

AR: Address Reference Input

O0 to O7: Outputs

$\overline{CE}$: Chip Enable

$\overline{OE}$: Output Enable

Vpp: +25V Program Supply

Vcc: +5V Supply

GND: Ground

$\overline{CE}$	$\overline{OE}$	AR	Vpp	Outputs	Mode
L	L	L	+5	DOUT	Read
H	X	L	+5	Hi-Z	Standby
⊓ H L	H	L	+25	DIN	Program
L	L	L	+25	DOUT	Program Verify
L	H	L	+25	Hi-Z	Program Inhibit

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Temperature Under Bias	T_{op}	0 to + 70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Program Voltage (Respect to Gnd)	V_{PP}	−0.3 to +28	V
Supply Voltage (Respect to Gnd)	V_{CC}	−0.3 to +6	V
Input Voltage (Respect to Gnd)	V_{IN}	−0.3 to +6	V
Output Voltage (Respect to Gnd)	V_{OUT}	−0.3 to +6	V
Power Dissipation	P_W	0.6	W

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.75	5	5.25	V	5V ± 5%
Program Voltage	V_{PP}	$V_{CC} - 0.6$		$V_{CC} + 0.6$	V	Read Mode
	V_{PP}	24.0		26.0	V	Program Mode
Input Signal Level	V_{IH}	2.2	5	6.0	V	Respect to Gnd
	V_{IL}	−0.1	0	0.8	V	
Operating Temperature	T_a	0		+70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 5%; V_{PP} = V_{CC} ± 0.6V; T_A = 0 to +70°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}			10	μA	V_{IN} = 5.25V/0.45V
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 5.25V
V_{PP} Current	I_{PP}			5	mA	V_{PP} = 5.85V
	I_{PP1}			6	mA	V_{PP} = 25V ± 1V, $\overline{CE}$ = V_{IL}, T_a = 25°C ± 5°C
	I_{PP2}			30	mA	V_{PP} = 25V ± 1V, $\overline{CE}$ = V_{IH}, T_a = 25°C ± 5°C
V_{CC} Current	I_{CC1}		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
	I_{CC2}		60	100	mA	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}
	I_{CC}			100	mA	V_{PP} = 25V ± 1V, T_a = 25°C ± 5°C
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{CC} must be supplied before or when V_{PP} is supplied, and must be cut off when or after V_{PP} is cut off.
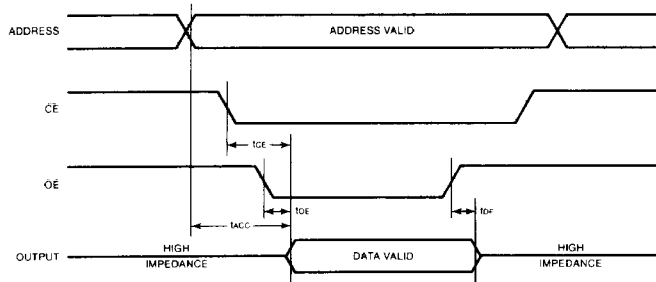
AC CHARACTERISTICS
READ MODE

(V_{CC} = 5V ± 5%; V_{PP} = V_{CC} ± 0.6V; T_A = 0 to 70°C unless otherwise noted)

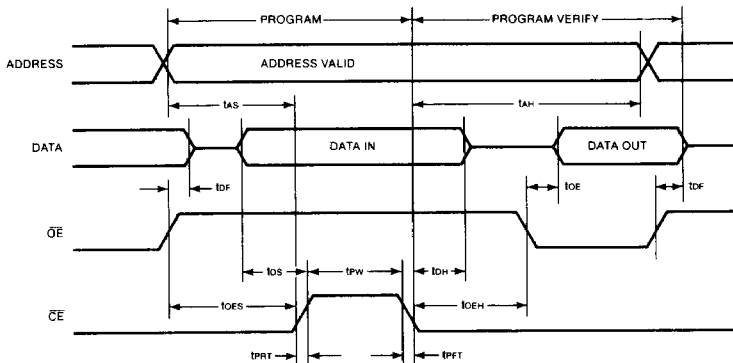| Parameter	Symbol	Min.	Typ.	Max.	Unit
Access Time	t_{ACC}		250	450	ns
Chip Enable to Output Valid	t_{CE}		280	450	ns
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float	t_{DF}	0		100	ns

READ MODE

Notes: 1. A Read occurs during the overlap of a low $\overline{CE}$ and a low $\overline{OE}$.
2. t_{ACC} is specified with $\overline{CE} = \overline{OE} = V_{IL}$.
3. t_{CE} is specified with $\overline{OE} = V_{IL}$.
4. Input Pulse Levels: 0.8V to +2.2V
5. Input Rise and Fall Time: 20 ns
6. Timing Measurements Reference Level: Input = 1.0V and 2.0V, Output = 0.8V and 2.4V
7. Output Load: 1 TTL Gate and C_L = 100 pF

PROGRAM MODE

$(V_{CC} = 5V \pm 5\%; V_{PP} = 25V \pm 1V; T_a = 25°C \pm 5°C$ unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Address Setup Time	t_{AS}	2			μS
$\overline{OE}$ Setup Time	t_{OES}	2			μS
Data Setup Time	t_{DS}	2			μS
Address Hold Time	t_{AH}	2			μS
$\overline{OE}$ Hold Time	t_{OEH}	2			μS
Data Hold Time	t_{DH}	2			μS
Output Disable Delay Time	t_{DF}	0		120	ns
Output Enable Delay Time	t_{OE}			120	ns
Program Pulse Width	t_{PW}	45	50	55	ms
Program Pulse Rise Time	t_{PRT}	5			ns
Program Pulse Fall Time	t_{PFT}	5			ns

PROGRAM MODE

Notes: 1. Programming occurs with $V_{PP} = 25V \pm IV$ during the overlap of a high $\overline{OE}$ and pulsed-high $\overline{CE}$.
2. Measurement conditions same as those for Read Mode. (Notes 4–7).

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## CAPACITANCE

$T_A = 25°C, f = 1$ MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output Capacitance	C_{OUT}			12	pF
Input Capacitance	C_{IN}			6	pF

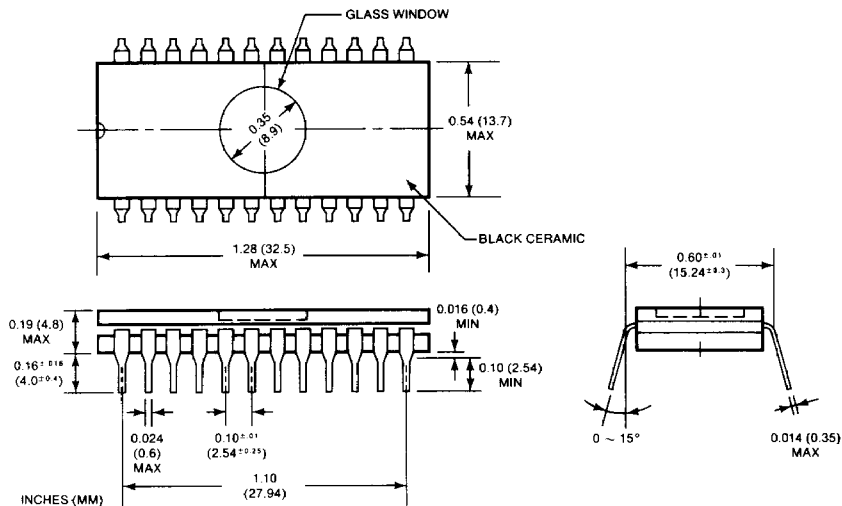**Note:** This parameter is periodically sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

PROGRAMMING: All bits of the EPROM are set to the "1" state at the time of delivery or after erasure. Data is introduced by selectively programming "0's" into the desired bit locations. The only way to change a "0" to a "1" is by ultraviolet light erasure.
ERASURE: The contents of the EPROM can be erased by irradiation of ultraviolet rays having a wavelength of 2537 Angstroms. The irradiation energy for erasure should be a minimum of 15W-sec/cm². The charge (electrons) in the floating gates decreases with irradiation time, but erasing time "tE" until reaching the threshold point (where all bits are sensed as "1's") is insufficient. Irradiate for another 2 × tE for sufficient discharge of electrons.
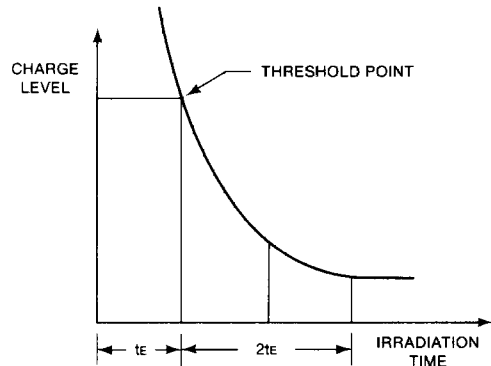
PACKAGE SPECIFICATIONS

24 LEAD CERAMIC (AS)