PLESSEY Semiconductors SL 600 series

Integrated Circuits for Radio Communications

2nd EDITION
Schutzgebühr
DM 5 inkl. 5,5% Mwst.

Applications Manual

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This manual was first published in 1972 to satisfy demand for applications information specific to the Plessey Semiconductors SL600 series integrated circuits.

Since then, new devices have been added to this versatile range of circuits and have therefore been incorporated into this, the second edition, together with some revision and rationalisation of the original material.

Feedback from users of the first edition has been invaluable to the compilation of the additional material – the author therefore wishes to express his gratitude to those who have contributed in this way and trusts that the second edition will prove to be as well received as the first.

J.M.B.

SL600 SERIES

Integrated Circuits for Radio Communications

APPLICATIONS MANUAL

James M. Bryant
Linear Applications Manager

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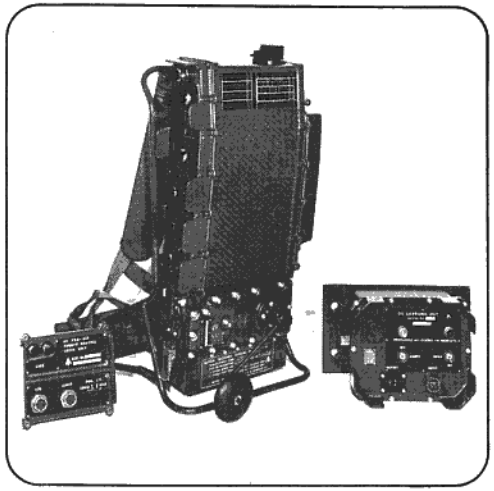


Designed and manufactured by Plessey Avionics and Communications, the Clansman UK/PRC 320 HF Manpack Transceiver makes extensive use of SL600 series integrated circuits. The transceiver operates in USB, LSB, AM and CW (narrow band) modes over a frequency range of 2 to 30 MHz

The Eudgert 'Diamond' high-performance HF Amateur Band Transceiver is an example of modern equipment designed for the radio amateur. The transceiver uses solid state circuitry – mainly SL600 series devices – in all but the transmitter PA stage.

Circuit Data 1

RF/IF Amplifiers SL610C,611C & 612C

The SL610C, SL611C and SL612C integrated RF amplifiers are similar circuits, having typical voltage gains of 10, 20 and 50 and upper 3dB gain points at 140MHz, 100MHz and 15MHz respectively. The first two draw a supply current of about 15mA at 6V and have some 50dB AGC range while the SL612C draws 3.5mA and has 70dB of AGC. All three are intended for use with +6V supplies and have internal decoupling. They will drive an output signal of about 1V rms.

The cross-modulation of the circuits is 40dB down on signal at 1V rms output with no AGC, and at 250mV rms input with full AGC. The input and output admittances of the circuits are not greatly affected by AGC level.

CIRCUIT APPLICATIONS

There are seven connections to each circuit: an input, an input bias point, an AGC input, the output, the positive supply pin and two earths – for input and output respectively.

The positive supply should be 6 volts, but the devices will function at supplies of up to 9 volts. Since internal HF supply decoupling is incorporated a certain amount of HF ripple can be tolerated in the supply. LF ripple should be kept down as it can cause inter-modulation – especially at large HF signal levels – and 10mV rms of LF ripple should be considered a maximum.

The AGC characteristic is shown in Fig. 1. It is temperature dependent, so that while a potentiometer may be used to provide a gain control voltage the gain so defined will not be temperature stable. The AGC terminal will normally draw about 200μA at 5V – in some SL610C and SL611C devices this may be as high as 600μA.

There are two earth connections: pin 4 is the input earth and pin 8 the output earth. When several devices are cascaded pin 8 of one stage and pin 4 of the next should have a common earth point – also high common earth impedances to pin 4 and pin 8 of the same device should be avoided. Fig. 2a shows a circuit where common earth impedance could cause instability and Fig. 2b shows one where the input and output signals have correct point earthing. If extra supply decoupling is used the capacitor should ground to the output earth point. The can may be separately earthed in applications at VHF or in the presence of a large RF field.

The input bias point (pin 6) is normally connected directly to the input (pin 5) and the signal applied through a capacitor but occasionally, when the signal is obtained from a tap on a coil, the arrangement in Fig. 2b may be used to give slightly improved noise performance.

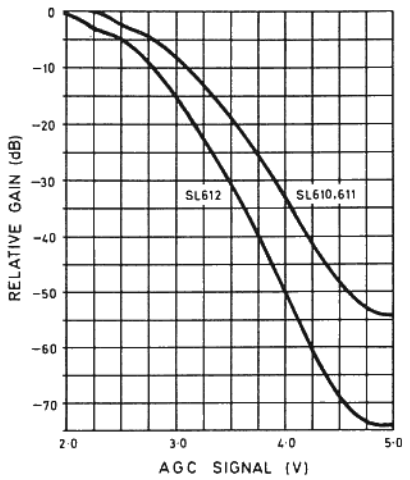


Fig. 1 SL610/11/12 AGC characteristics

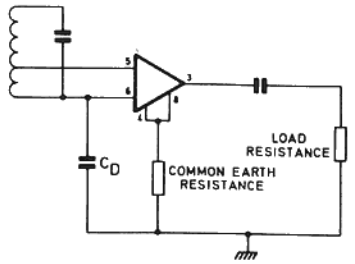
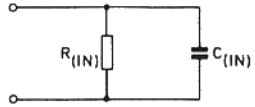


Fig. 2(a) Incorrect connection of earths



(a) Input circuit

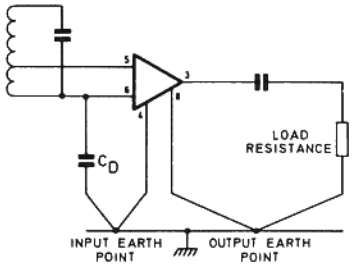
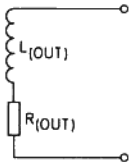


Fig. 2(b) Correct connection of earths



(b) Output circuit

Fig. 3 Equivalent circuits

C_D is a decoupling capacitor. The SL610/611 noise figure is approximately 4dB at 300Ω source impedance and 6dB at 50Ω and at 2.5kΩ; the noise figure for the SL612 is 3dB at 800Ω source impedance.

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output respectively are shown in Figs. 3a and 3b and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Figs. 4 and 5. It will be seen that for the SL610C and the SL611C, R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL612C, R_{in} is not negative and R_{out} is negative only below 700kHz.

If an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and R1 is higher than R_{in}. Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of

L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input is inductive, therefore, it may be shunted by a 1k resistor; where the load is capacitive, 47Ω should be placed in series with the output.

Suitable input arrangements for the amplifiers are shown in Fig. 2b and Fig. 6. The method shown in Fig. 6a is representative of all inputs – the input and bias points are directly-connected and the signal is coupled via a capacitor. If the input is inductive the 1k resistor shown in Fig. 6b may be required, although usually it can be omitted. If a crystal filter is used and the terminating impedance of the IC is correct it may be connected directly to the circuit. Otherwise the filter should be correctly terminated, allowing for the impedance of the IC, and coupling made via a capacitor.

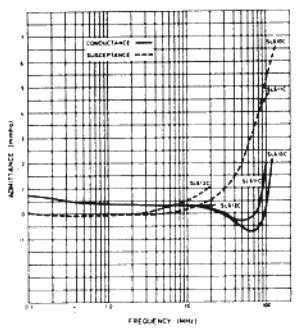


Fig. 4 Input admittance with o/c output (G_{11})

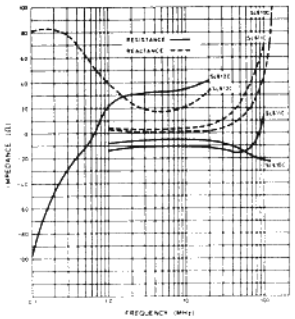
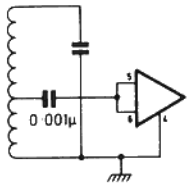
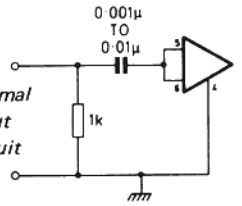


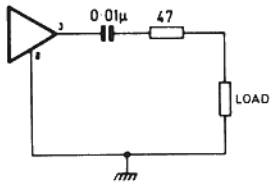
Fig. 5 Output impedance with s/c input (G_{22})



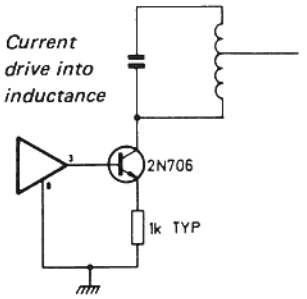
(a) Tuned circuit



(b) Normal input circuit



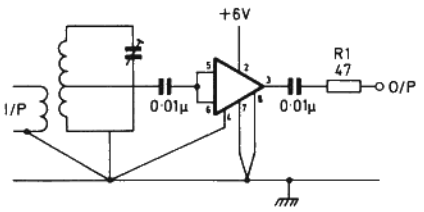
(c) Normal output circuit



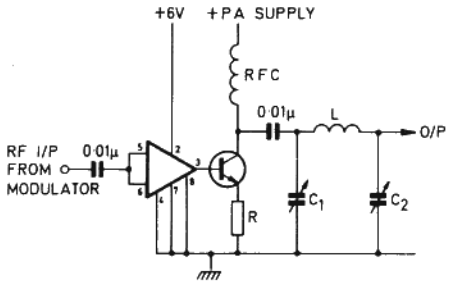
(d) Current drive into inductance

Fig. 6 Input and output circuits

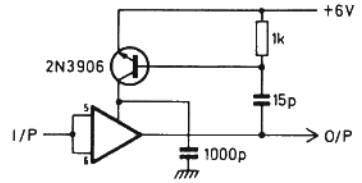
The output is a voltage source, with the impedance characteristics mentioned above. Output coupling is via a capacitor, with a series resistor if necessary to preserve stability (Fig. 6c). If a current output to a tuned circuit is required the arrangement in Fig. 6d is suitable, using almost any small signal NPN transistor with an f_T of over 300MHz and low C_{OB}. To drive particularly low impedances, e.g. a 50Ω coaxial cable, this impedance should be increased somewhat by a series output resistor (say, 100Ω) as, if the output is loaded directly by low impedance, most of the negative feedback will be removed – with consequently poor linearity and constancy of gain. Examples of the use of these amplifiers are shown in Fig. 7.



(a) *RF preamplifier. Use SL610C up to 140MHz, SL611C up to 70MHz, SL612C up to 12MHz. R1 may be omitted if the load is neither capacitive nor very low impedance.*



(b) *Linear power amplifier for low power SSB transceivers. L, C1 and C2 form the output π tank circuit. The values of PA supply and R should be chosen to suit the transistor used.*



(c) ***Constant level RF amplifier stabilising at approximately 500mV r.m.s output over a range of inputs greater than 20dB. SL610C, 611C or 612C may be used. With tuned feed-back, this circuit makes an excellent constant level oscillator.***

Fig. 7 SL610/11/12: typical applications

Limiting RF Amplifier / Detector SL613C

The SL613C is a simple but versatile circuit consisting of a broadband amplifier with execellent limiting characteristics, and a simple transistor detector. The broadband amplifier has 3dB points of 5 and 150 MHz, a 4.5dB noise figure, and a gain of 4. The detector starts operating with an input of about 10mV r.m.s. and limits, with the main amplifier, at 120mV r.m.s. input, when the detected output current is about 1mA. The circuit, which has internal bias and supply decoupling, consumes 15mA at 6V supply.

CIRCUIT DESCRIPTION

The circuit diagram of the SL613 is given in Fig. 8. The limiting amplifier consists of the long-tailed pair of transistors, TR1 and TR2, the output of which drives an emitter follower output stage, the detector and the other input of the long-tailed pair via a potential divider to provide negative feedback. The potential divider defines the gain of 4, and the 330pF DC blocking capacitor defines the low frequency 3dB point of 5 MHz. Careful design of both the long-tailed pair and the bias and feedback circuitry ensures that the amplifier limits symmetrically.

The detector consists of TR4 and TR5 (a matched pair) and the output current appears on the collector of TR5. There is a small leakage current of about 30µA with no signal input.

CIRCUIT APPLICATIONS

Fig. 9a shows the SL613C used as an amplifier and detector. Only two capacitors and a resistor are used, pins 1 and 8 are connected together internally to the case of the device and to the output earth. If possible both should also be connected together externally to minimise lead inductance. Pin 5 is the input earth. The rules concerning the input and output earths of the SL610/11/12 (pp 3 & 4) apply equally to the SL613C. Power is connected to pin 2 and should be between +6V and +7.5V and free of LF ripple; small amounts of HF ripple will be removed by the internal HF decoupling

Pin 3 is the RF output and has an output impedance of about 35Ω and 3pF. It must always be isolated at DC by a capacitor and should not be required to drive a capacitive load of over 10pF, or a resistive load of under 50Ω, without a buffer resistor of about 50Ω. While instability is unlikely if this precaution is neglected, it is possible and in any case the response of the SL613C is severely affected.

The detected output on pin 4 is a current flowing out of a transistor collector. The pin must always be biased between +3V and +9V, even if the detector output is not used. In this latter case pins 2 and 4 are generally connected together. There is normally a small leakage of some 30µA with no signal, which rises quite linearly to 1mA at 120mV r.m.s. input, at which point the amplifier limits and the detected output no longer increases with signal input. This detector was designed as an AGC detector but may be used quite successfully as an AM envelope detector provided that the signal is not more than 90% modulated and does not limit the amplifier on positive peaks.

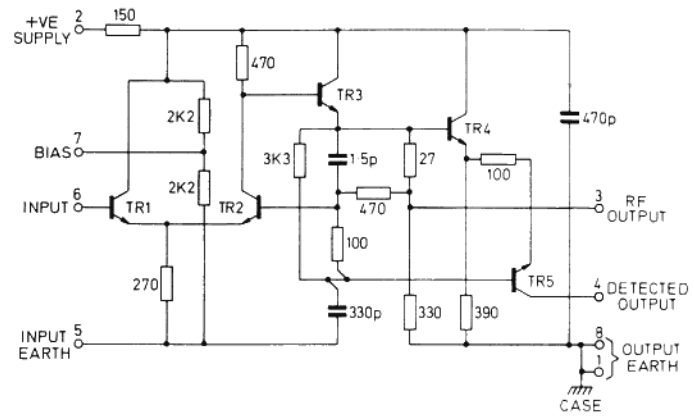


Fig. 8 SL613C circuit diagram

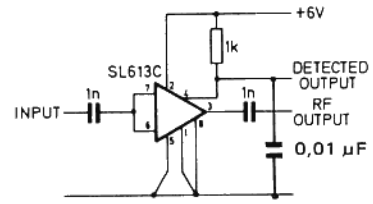
Pin 6 is the signal input. It is normally connected directly to the bias pin, pin 7, but may be used, like the SL610/11/12 input pin, in the circuit shown in Fig. 2b, i.e. with pin 7 connected to the 'cold' end of a coil and decoupled to earth and pin 6 connected to the 'hot' end of the coil. The impedance of the input pin alone is 5kΩ and 6pF but if it is connected to pin 7 this falls to 800Ω and 8pF. Inputs of over 1.5V r.m.s. will overload the limiting amplifier and should be avoided.

The gain from pin 6 to pin 3 is 4 (12dB) and the noise figure, with a source impedance of 500Ω, is 4.5dB. The amplifier limits when the input exceeds 120mV r.m.s.

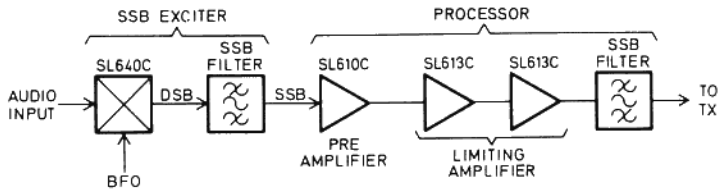
Typical uses of the SL613 are shown in Figs 9b and 9C. They consist of a speech processor for SSB transmitters which can increase the average/peak power ratio by up to 12dB and an auxiliary AGC system for AM receivers using a SL621 speech AGC system.

The SSB processor in Fig. 9b consists of two SL613C's, an SL610C and a SSB filter. A SSB signal is produced in one of the usual ways (in this case by the filter method), amplified by the SL610C and fed to two cascaded SL613C's. These clip the signal but, because of their excellent symmetry, preserve the zero-crossing points. The resulting signal consists of the required clipped SSB signal together with harmonics and intermodulation products which are removed in a SSB filter, leaving only the clipped SSB which is then transmitted. This system has little effect on intellegibility (although it alters voices somewhat) and improves the mean/peak power ratio of a normal SSB signal by up to 12dB. A danger of adding such a system to an existing SSB transmitter is that the increased power may cause damage to inadequately designed linear amplifiers, but if this is not a problem the increase in effective power for the same amplifier power is well worth the cost of the extra filter and integrated circuits.

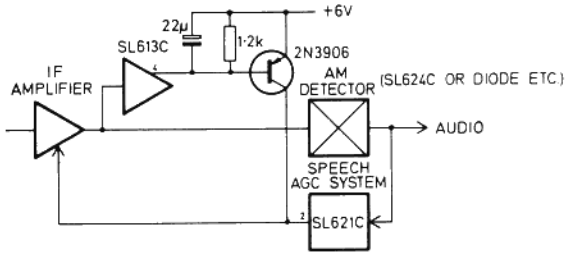
The carrier AGC system in Fig. 9c is normally inoperative since a small modulated signal will supply the SL621C with sufficient audio to maintain AGC. If the modulation is removed the SL621C will provide no AGC and the carrier level rises until the detected current in the SL613C turns on the PNP transistor (a 2N3906 is shown but any small Si PNP type will suffice) and provides AGC again, preventing the IF amplifier from limiting.



(a) An amplifier detector



(b) Signal processor for SSB transmitters



(c) Carrier supplementary AGC system for AM receivers using SL621C speech AGC

Fig. 9 SL613C applications

AGC Generators SL620C, SL621C

The SL621C is an audio-operated AGC generator designed for use with the SL610/11/12 RF amplifiers in SSB receivers. The SL620C, designed to provide AGC to the SL630C audio amplifier, is exactly similar in operation to the SL621C and is, therefore, not separately described in this section (but see pages 28 and 29).

An ideal single sideband AGC generator must set the AGC rapidly when a new signal appears and follow a rising or fading signal but, if the signal disappears altogether (as in pauses in speech), retain the AGC level until the signal recommences. If the signal remains absent for more than a preset time, however, the system should rapidly revert to full gain. The SL621C will perform these functions and will also produce short-lived pulses of AGC to suppress noise bursts.

CIRCUIT DESCRIPTION

The operation of the circuit is described with reference to the circuit diagram (see Technical Data), and Fig. 10, which illustrates the dynamic response of a system controlled by an SL621C AGC generator.

The SL621C consists of an input AF amplifier, TR1—TR4, coupled to a dc output amplifier, TR16—TR19, by means of a voltage back-off circuit, TR5, and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

An audio signal applied to the input rapidly establishes an AGC level, via TR14, in time t_1. Meanwhile the long time constant detector output (TR15) will rise and after t_3 will control the output because this detector is the more sensitive. If the signals at the SL621C input are greater than approximately 4mV rms they will actuate the trigger circuits TR6—TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate which corresponds to a rise in receiver gain of 20dB/sec. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely, as in pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector (TR14) falls to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, thus holding off TR12 via TR11. When the pulses cease, C3 discharges and after t_5 turns on TR12, rapidly discharging C2 (in time t_4) thus restoring full receiver gain. The hold time, t_5, is approximately one second with C3 = 100μF. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses. Fig. 10 also shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

The various time constants quoted are for C1 = 50μF and C2 = C3 = 100μF. These time constants may be altered by varying the appropriate capacitors.

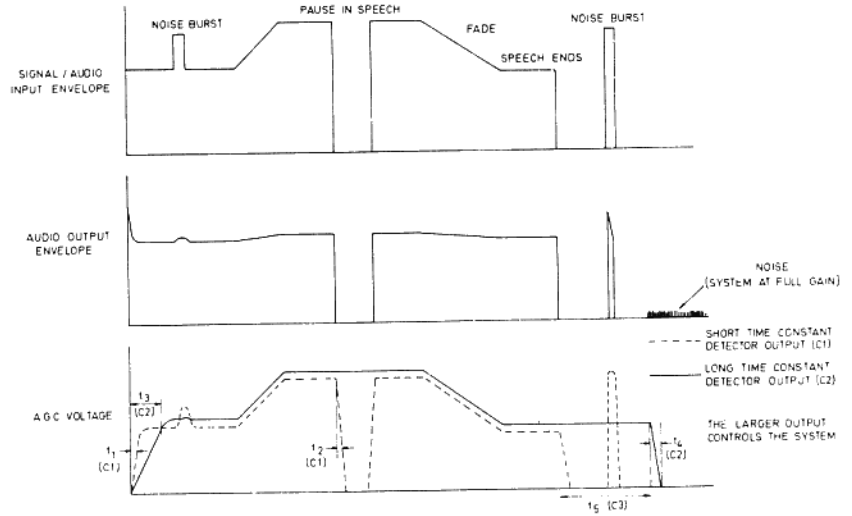


Fig. 10 Dynamic response of a system controlled by an SL621C AGC generator.

CIRCUIT APPLICATIONS

The SL621 is used in an SSB receiver as shown in Fig. 11. AGC need only be applied to two of the gain stages even if there are more than two such stages in the receiver since AGC applied to two stages only will result in over 120dB AGC range. It is usual to apply AGC to the first RF stage and the first IF stage and it will be seen from Fig. 12 that an SL612 IF amplifier reacts earlier to an increasing AGC voltage than an SL610C RF amplifier. This has the effect of delaying the AGC to the input stage, thus improving the receiver signal to noise ratio at low AGC levels.

Fig. 12 also shows the total attenuation to be expected at any AGC voltage when AGC is applied to one SL610C and one SL612C in a system; from this one can calculate the calibration of an 'S' meter for use with the SL621C. Such a meter, as shown in Fig. 11, should have a sensitivity of 2.6V FSD and be calibrated linearly from 0 to 120dB.

The output current capability of the SL621 is not high and it should not be expected to drive more than three SL610/11/12 devices in addition to an 'S' meter circuit similar to that shown in Fig. 11.

There are two other important points to observe when using the SL621C: supply de-coupling and input coupling. Since capacitors C1 and C3 may need to charge very quickly

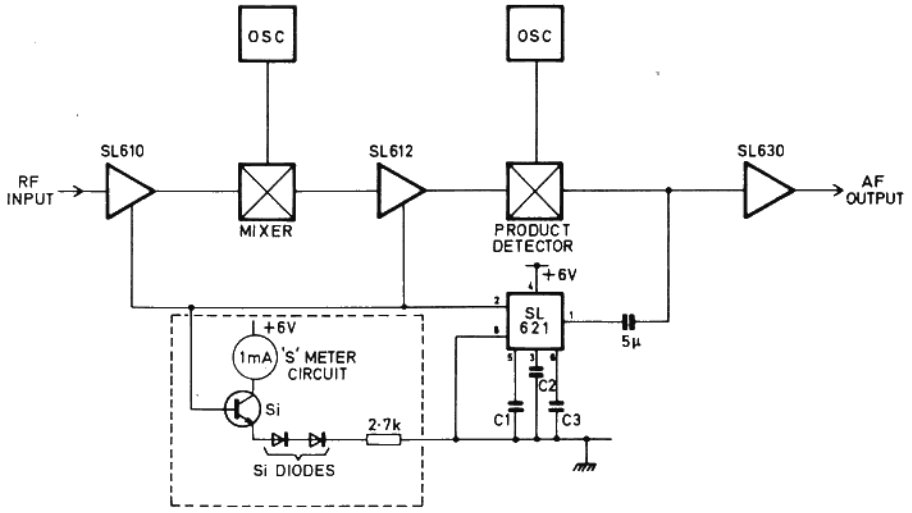


Fig. 11 An SL621C used to control an SSB receiver.

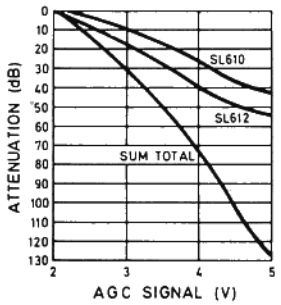


Fig. 12 Attenuation v. AGC signal.

the source impedance of the 6V supply line at low frequencies should be very low, if necessary being decoupled by a low impedance 1000µF capacitor placed near the SL621C. The input to the SL621C must be supplied through a capacitor having a reactance of 470Ω at the lowest input frequency to be used.

In the presence of RF fields the AGC line may need to be decoupled: a 5000pF capacitor from pin 7 of each RF amplifier to earth and a 100Ω resistor from each pin 7 to the AGC line should be adequate. It is, however, important not to use a capacitance greater than 15000pF,otherwise the impulse suppression characteristic of the circuit will be degraded.

The SL621 may be used with supply voltages between +6V and +9V.

AF Amplifier, VOGAD, & Sidetone Amplifier SL622C

The SL622C integrated circuit is an audio amplifier with internal AGC designed to provide a constant output of 100mV rms from a 60dB range of input. The amplifier has an open-loop gain of 52dB, and the device also incorporates a sidetone amplifier with 29dB gain which limits when the input exceeds 50mV p-p.

Applications exist for the SL622C wherever microphones are used: transmitters, intercommunication systems and telephone systems are obvious examples. The SL622C can also be usefully employed in radio receivers (in addition to the normal receiver AGC) to stabilise audio output.

CIRCUIT DESCRIPTION

The circuit (Fig.13) is in four sections: main amplifier, sidetone amplifier, AGC system, and voltage regulator. The balanced input (pins 5 and 6) is applied in parallel to both the main amplifier and the sidetone amplifier. The sidetone amplifier consists of two balanced long-tailed pair stages, the second of which is a limiting stage, followed by an emitter follower output stage. The main amplifier consists of two separate sections; the first is a balanced input section consisting of long-tailed pair amplifiers and gain-controlled stages. The input section has a single-ended output to the second section, comprising the output stage. The output stage has external connections for the application of frequency-shaping and threshold control, and also drives the detector which generates the AGC. An on-chip voltage regulator allows the device to be operated from any supply between +6V and +12V, and is a simple series stabiliser giving a +4.7V line in the chip from which the rest of the circuit is operated. Supply ripple at +6V is attenuated by −26dB, a figure which rises with increasing supply voltage. A typical application is shown in Fig. 14.

CIRCUIT APPLICATIONS

The Voltage Regulator

The power supply is connected to pin 1; pin 3, which may be decoupled at LF to reduce supply ripple and improve sidetone linearity, is the +4.7V stabilised supply. It is recommended that pin 3 also be decoupled at HF by a 0.05µF capacitor. Some users of the SL622 may wish to take small currents from pin 3 to other circuits requiring a stabilised supply. Whilst this is unlikely to harm the circuit if only one or two milliampères are taken, the device may not perform to full specification. The current consumption of the integrated circuit rises from 14mA at 6V to 24mA at 12V.

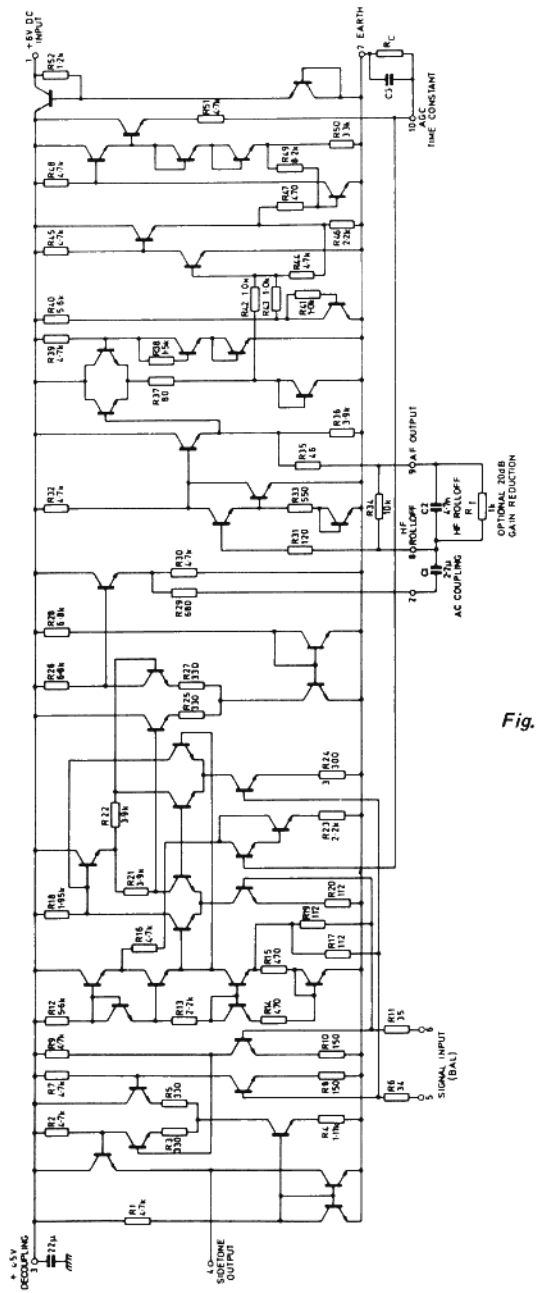


Fig. 13 SL622C circuit diagram

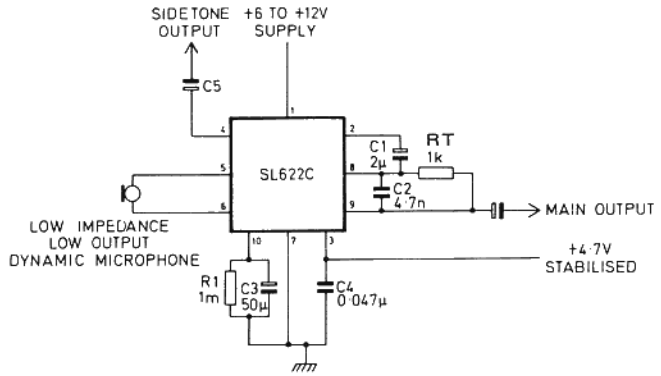


Fig. 14 The SL622C used as a microphone amplifier

Main Amplifier

An external capacitor, C1, connects the output of the front end of the AGC controlled amplifier (pin 2) to the output stage (pin 8). This capacitor defines the lower 3dB point of the main amplifier and its value – which is inversely proportional to frequency – must be chosen accordingly. For example, a lower frequency limit of 300Hz would require a value of 2µF. If a polar capacitor is used, its positive lead must be connected to pin 2.

Similarly, the HF 3dB point of the main amplifier is governed by C2, connected between pins 8 and 9, and by R_T, the value of which determines the threshold at which AGC commences. For a given value of R_T, C2 is inversely proportional to frequency. Table 1 shows values of threshold voltage, R_T and C2 for an upper cut-off frequency of 3kHz.

Threshold voltage (mV rms)	R_T (Ω)	C2 (µF)
0.1	Open circuit	.005
1.0	1,000	.05
10	100	.5

Table 1

The output impedance of the main amplifier is 50Ω. As the output is taken from an emitter follower it should not be used to drive capacitive loads. The output when AGC is operating is just under 100mV rms.

Sidetone Amplifier

The sidetone output is taken from pin 4 and is not frequency-shaped. The output impedance is 200Ω and, like the main output, the sidetone output should not be used to drive capacitive loads.

The balanced input (pins 5 and 6) may be used as a differential input (in which case the input impedance is 300Ω and the two inputs may have a dc path between them) or a single-ended input can be applied to one pin while the other is decoupled to earth. In the latter case the input impedance is 180Ω. Balanced inputs may be as high as 375mV p-p but single-ended inputs should not exceed 50mV p-p. When a balanced input is used, the common-mode rejection of the amplifier is over 30dB.

The problems associated with amplitude distortion inherent in simple VOGAD circuits have been largely overcome in the design of the SL622C. In certain circumstances, however, some distortion of the leading edge of the first spoken syllable can occur, but only after a considerable pause in speech. The effect is due to overshoot, which in turn results from capacitor C2 being allowed to discharge below the AGC threshold. In most applications however, the distortion is not of sufficient significance to justify the additional circuitry necessary for its elimination.

Since the device has only one earth connection for both input and output, care must be taken to avoid high impedance earth connections which might cause instability. In conditions where high RF fields may be encountered the can should be separately earthed to pin 7 or to a ground plane.

AGC System

A resistor and capacitor (C3, R1), connected in parallel between pins 7 and 10, set the AGC attack and decay times. The attack time constant is proportional to the value of the C3 and is 0.4ms per μF; the decay rate is inversely proportional to the time constant (C3 x R1) of the two components and is 20dB/sec for a time constant of 50sec. The value of R1 should lie between 470 kΩ and 1.5MΩ, and C3 should exceed 5μF. The usual values when the SL622C is used in speech systems are 1MΩ and 50μF: this gives 20ms attack time and 20dB/sec decay rate.

External Gain Control

Since the gain control voltage range of the SL622C is very small it is not really practicable to use the device as a VCA by applying a control voltage to pin 10. However, the device can be easily muted by connecting pin 10 to +4V or held at full gain by earthing pin 10. Some provision must be made for discharging C3 when the muting voltage is removed or the muting period will be prolonged until the capacitor has discharged through R1 (Fig. 14).

AM Detector, AGC Amplifier and SSB Demodulator SL623C

The SL623C is one of the most complex of the SL600 family of integrated circuits and has been developed for use at frequencies of up to 30MHz in radio communications equipment. It consists of an AM detector, an SSB detector and an AGC generator designed for use with AM. The SL623C was introduced to enable the small-signal sections of an HF AM/SSB transceiver to be completely integrated – all functions with the exception of the power amplifier can be realised with SL600 series integrated circuits. The outputs of the SL623C will drive most audio output stages with input impedances over 1 kΩ, and are particularly suitable for driving either the SL630C or the SL414A

In addition to its audio outputs, the SL623C AGC generator is designed to control SL610/11/12 RF/IF amplifier strips, but, unlike the SL621C AGC generator, which operates from an audio signal, the SL623C control voltage is carrier-derived. It is therefore less suitable for use with SSB or CW. However, the AGC output pins of an SL621C and an SL623C may be connected together for an SSB/AM receiver, the gain then being controlled by the device with the higher output voltage.

CIRCUIT DESCRIPTION (Fig. 15)

The IF input is applied directly to one input of a full-wave detector and, via a unity-gain inverting amplifier, to the other input of the full-wave detector and to the signal input of a balanced demodulator. Two outputs from the full-wave detector are brought out of the package: audio (pin 1) and AGC (pin 2). The AGC signal is used as the input to the AGC amplifier of the device. The AGC amplifier consists of two amplifiers in series – the first has a gain which may be varied between −0.25 and −5 by an external resistor connecting pin 2 to pin 5 and the second has a fixed gain of −20 and a frequency compensation point. The SSB detector, which requires a carrier input of 100mV rms, consists of a simple balanced demodulator.

A single positive supply of between +6V and +9V is required. The supply should be decoupled close to the can by a 0.1μF capacitor connected between pins 7 and 10. Current consumption is approximately 10mA at 6V supply and zero AGC voltage, but rises with both supply voltage and AGC output level

CIRCUIT APPLICATIONS

AM Detector

The detected AM output on pin 1 has an output impedance of about 1kΩ and should

be decoupled at RF with a 0.01μF capacitor (C1). It should be connected to the audio stage via a dc blocking capacitor. Pin 2 is an output similar to that at pin 1 but should be decoupled with a 50μF capacitor (C2) to remove AF, and connected via a preset potentiometer R28 to the AGC amplifier input (pin 5) to provide rectified carrier for amplification as AGC. C1 and C2 should be connected directly to the earth pin (10) via the shortest possible leads, which should not be common to any other components. C2 should have an AF series resistance of under 1Ω and, if it does not also have a low RF impedance, should be shunted by a 0.01μF RF bypass capacitor (C3). These measures prevent instability due to possible RF current loops.

AGC Generator

Pin 3, the AGC amplifier phase correction point, should be decoupled to pin 10 by a 1μF capacitor (C4), keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

The AGC output (pin 4) will drive at least two SL610/11/12 amplifiers and the 'S' meter circuit shown in Fig. 11. The SL623 AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623C will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from pin 8 to pin 1. Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets, different filters are used for AM and SSB; these will also need to be switched.

The 10kΩ gain-setting preset potentiometer R28 is adjusted so that a dc output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL623C for a 4dB increase in input.

SSB Demodulator

The carrier input is applied to pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the dc level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01μF capacitor. The output impedance of the detector is 3kΩ and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs — no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the

detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting pin 8 of the SL623C to pin 1 of the SL621C via a 2kΩ resistor in series with a 0.5μF capacitor.

Input Conditions

The input impedance at pin 9 is about 800Ω in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the dc bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

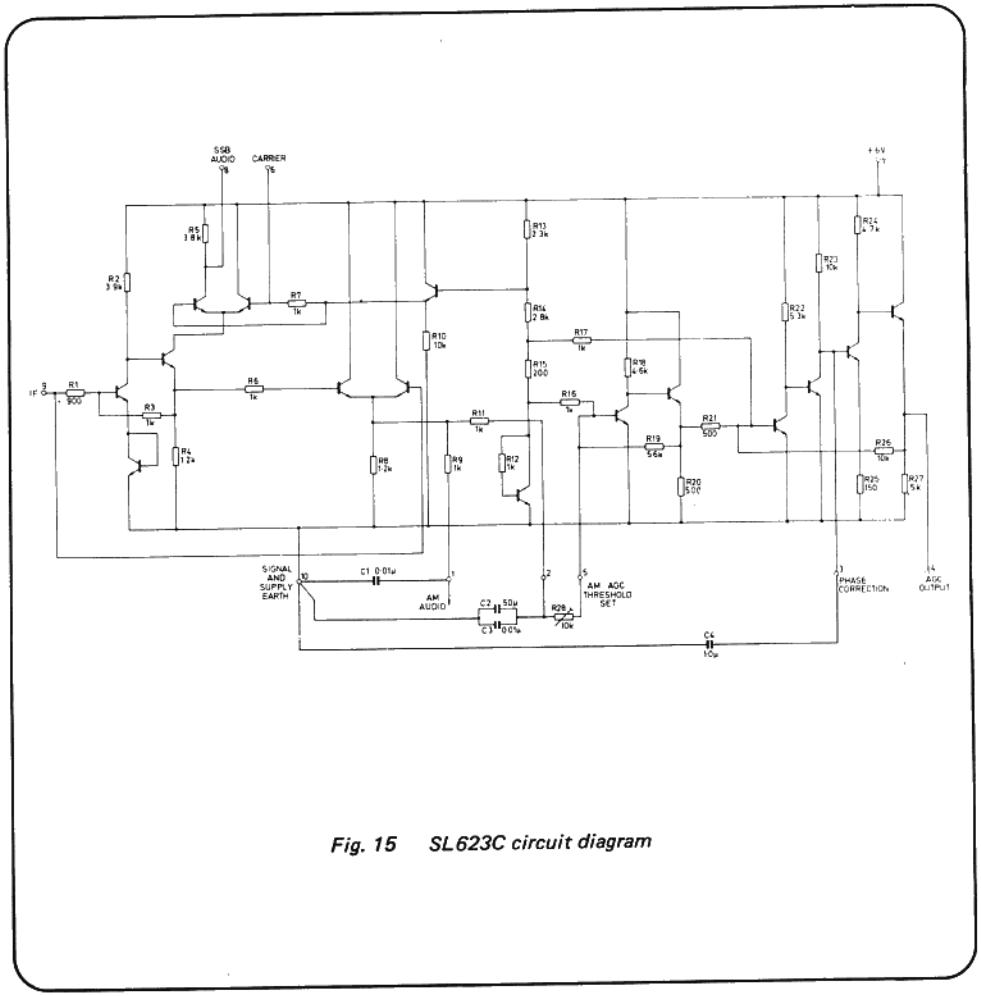


Fig. 15 SL623C circuit diagram

Multimode Detector SL624C

The SL624C is a new member of the SL600 family and has been introduced to meet the very heavy demand for a single integrated circuit capable of demodulating all the common types of radio telephony — SSB, AM and FM. The SL624C amply satisfies these requirements and also contains an audio amplifier with voltage-variable gain capable of driving a simple output stage of several watts. Although it detects the modulation of the modes mentioned above the SL624C does not incorporate an AGC output, so it is normally used in conjunction with an SL621 and an SL613C to give AGC both on audio for SSB reception and on the carrier for AM and FM.

CIRCUIT DESCRIPTION (See Technical Data)

The SL624C multimode detector consists of a double-balanced modulator and a five-stage balanced limiting amplifier. There is also an audio amplifier, with voltage-variable gain, connected directly to the double balanced modulator output, and a separate audio amplifier with a voltage gain of 4 and a medium power output intended as an audio driver. The circuit requires a single positive supply of between +9V and +12V, which must be capacitively decoupled at RF. Current consumption varies with audio gain and also with the value of the output resistor on pin 15 but is in the region of 20mA at 12V. The circuit is useable at frequencies up to 30MHz.

The circuit functions as a quadrature detector of FM with the output of the limiting amplifier (which is driven by the receiver IF strip) applied via an LC phase shift network to the external input of the double-balanced modulator. Since the output of a double-balanced modulator is proportional to the phase difference between the inputs, the system acts as an FM detector. For good limiting a signal of about 200μV is required at the limiting amplifier input.

For AM the circuit acts as a synchronous detector. The output of the IF amplifier is applied to the limiting amplifier and to the modulator signal inputs. Since the carrier is separated from the modulation in the limiting amplifier, both carrier and signal are applied to the modulator, which therefore demodulates the signal. The input to the limiting amplifier should be greater than 2mV r.m.s., with not more than 97% modulation, to ensure that limiting occurs even on modulation troughs. A similar detector is used for SSB; the signal is applied to the external modulator input and the limiting amplifier is used as a BFO.

Considerable switching is necessary to switch between modes, particularly between FM and AM/SSB. Since the SL624C is not particularly expensive it is better to use two SL624Cs in a multimode receiver: one for FM, the other for AM/SSB. Whilst not absolutely necessary, this method is certainly less expensive in components and simpler in layout than using one IC for all three modes.

CIRCUIT APPLICATIONS

In view of the different systems in which the SL624C may be used this section is divided into two parts — circuit connection details and system details.

CIRCUIT CONNECTIONS

The positive supply is connected to pin 2 and pin 5 is earth. The supply must be decoupled within 2mm of pins 2 and 5 by a good quality, short-lead 0.1μF capacitor. The supply voltage can be between 9 and 15 volts although at voltages above 12V dissipation can cause problems at high ambient temperatures.

Audio Amplifier

This amplifier has a voltage gain of 12dB (4 times) between the input on pin 1 and the outputs on pins 15 and 16. The input resistance at pin 1 is about 50kΩ and signals should be applied through a capacitor. The output impedance at pin 16 is 4kΩ and the DC potential is approximately half the supply voltage.

Pin 15 is the free emitter of an emitter follower with its base connected to pin 16. An external load resistor must be connected if the emitter follower is to be used. The output impedance at pin 15 can be as low as a few tens of ohms so the output can drive very simple output stages directly. Such an output stage is illustrated in Fig. 16. For output stages running on lower voltages slightly more complexity is necessary.

Limiting Amplifier

The limiting amplifier inputs are pins 3 and 4 and its outputs pins 6 and 7. It consists of five cascaded long-tailed pairs and is biased by DC feedback from pin 7 to pin 4 and from pin 6 to pin 3. This is accomplished as shown in the Fig. 17.

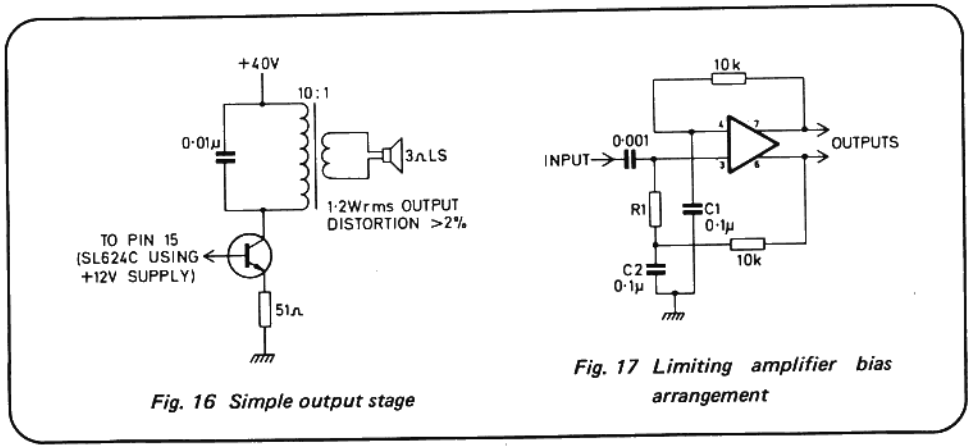


Fig. 16 Simple output stage

Fig. 17 Limiting amplifier bias arrangement

All the leads involved should be as short as possible and C1 and C2 must be earthed as close to each other and to pin 5 as possible to prevent instability due to RF earth currents. R1 can be any convenient value from 10Ω to 10kΩ and serves to prevent the input to the amplifier being earthed by C2. The input can also be applied to pin 4 if this is more convenient in which case R1 would be placed between C1 and pin 4. If a balanced input is required two resistors are necessary.

The limiting amplifier can handle signals up to 30MHz and limits with inputs of over 100μV r.m.s. As the gain varies with temperature, signals of about 300μV r.m.s. are required to ensure limiting at temperatures from −55°C to +125°C.

The open loop gain of the amplifier is about 70dB. When considered with its 30MHz bandwidth it is evident that great care must be taken to separate the input and output circuits to prevent instability. Another measure to prevent instability is to ensure that pins 6 and 7 are not loaded with less than 2kΩ of resistance or more than a few picofarads of capacitance.

Double-Balanced Modulator

This part of the circuit is essentially similar to the SL640C. The limiting amplifier outputs drive the carrier inputs of the modulator and are also brought out on pins 6 and 7 but it must be noted that these terminals must not be used for injecting a carrier signal from an external source. The signal inputs, connected to pins 8 and 9, have an input impedance of 2kΩ plus 3pF each and are internally biased. It is quite permissible to have a DC path between pins 8 and 9 but it is not necessary; there should be no DC path from either pin to any other point, however. Signal inputs to the modulator may be balanced or unbalanced; in the first case the signal is applied to pins 8 and 9 in antiphase, in the second one of the pins is decoupled to earth by 0.1μF while the other has the signal applied to it.

As explained in the SL640 circuit data the output of a double-balanced modulator with two signals at frequencies f_1 and f_2 applied to it consists of two frequencies: $|f_1 + f_2|$ and $|f_1 - f_2|$. In the normal use of the SL624C $|f_1 + f_2|$ will be several MHz and $|f_1 - f_2|$ will be an audio signal. The earlier the RF signal is eliminated the less likely it is to produce undesirable effects; a capacitor of 0.01μF or so connected within 2mm of pins 10 and 11 should be sufficient. This capacitor also produces 6dB/octave audio roll-off above 3kHz.

Audio Gain Control Stage

The audio gain control circuit is internally connected to the modulator. As the voltage on pin 13 increases from a reference voltage (pin 14) to 12V the gain of this stage increases by 80dB. The resistance at pin 13 is 5kΩ and the output impedance of the stage (pin 12) is 3kΩ. This stage may be used in either or both of two modes:as a muting stage or as a volume control. When used only as a mute, pin 13 is connected to earth when the audio is to be muted, otherwise to +12V. This may be done electronically by a squelch system or by a switch.

The volume control system uses a 47kΩ log potentiometer between pins 2 and 14 with the wiper connected to pin 13, a system which gives an approximately logarithmic gain control law. To achieve both volume control and mute the positive side of the potentiometer must not go directly to pin 2 but to the positive supply via the mute switch, (whether electronic or manual).

DETECTOR SYSTEMS

Four systems are described: FM, AM, SSB and AM/SSB switched. A squelch circuit useful for AM and FM reception and AGC systems useable with all three modes will also be described.

FM Detector

An FM detector is shown in Fig. 18. Basically, the signal is fed to the limiting amplifier and then, via a frequency-sensitive phase shift network, to the modulator. Since the output of the modulator is proportional to the relative phase of its two inputs, and since the phase of the external input, having passed the phase shift network, is proportional to frequency, the system acts as an FM detector.

The system illustrated operates at 10.7MHz; to operate at other frequencies, L, C1, C2 and C3 must be scaled accordingly. The circuit can be used at frequencies from 445kHz to 30MHz, but it may be necessary to introduce a resistor between pins 8 and 9 to reduce the Q of the phase shift network if $\Delta f/f$ (the percentage deviation) becomes too great. The detector may thus be used for commercial FM broadcast reception or for television sound sub-carrier demodulation.

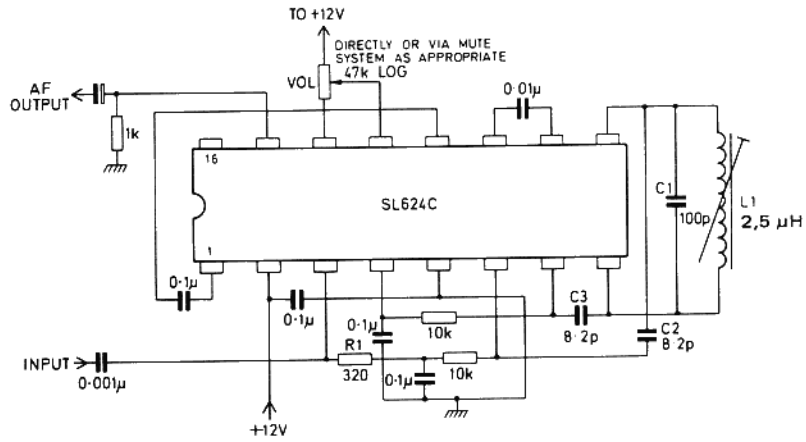


Fig. 18 FM detector

An input of at least 100μV r.m.s. is required, but 200μV r.m.s. or above is preferable. If an impedance match is required for any reason, R1 may be any value between 10Ω and 10kΩ.

The only adjustment required is the tuning of the phase-shift circuit. An FM signal of the correct centre frequency and with as large a deviation as the system is expected to handle is applied and the tuned circuit adjusted to obtain an undistorted audio output. There are three possible settings of this adjustment since the phase-shift characteristic has an S-Curve. The centre one of the three should be used since, although it may give a lower output than the other two, it will be least distorted and best able to survive long-term ageing of components.

The output will be high level noise if the limiting amplifier has insufficient input and does not limit. To prevent this condition, the squelch circuit shown in Fig. 19 is used. This circuit detects the limiting amplifier output and, if modulation is present (indicating that the amplifier is not limiting), mutes the detector audio stage. The squelch can be used with both the FM and AM detectors but not with the SSB detector.

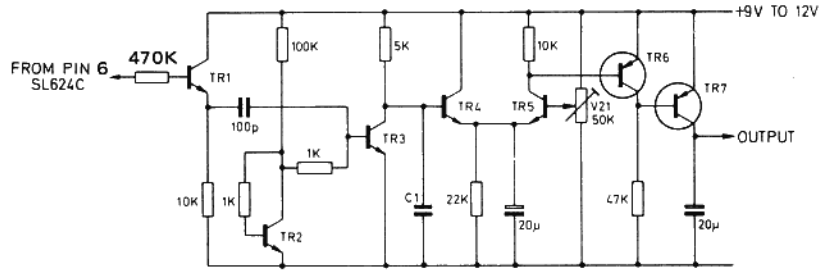


Fig. 19 Squelch system. Note: TR1 to TR5 is a Plessey SL3045 5-transistor array (discrete transistors are not suitable), TR6 and TR7 are discrete PNP types; C1 should be between 100pF and 5000pF, depending on permissible system noise; VR1 sets the squelch level

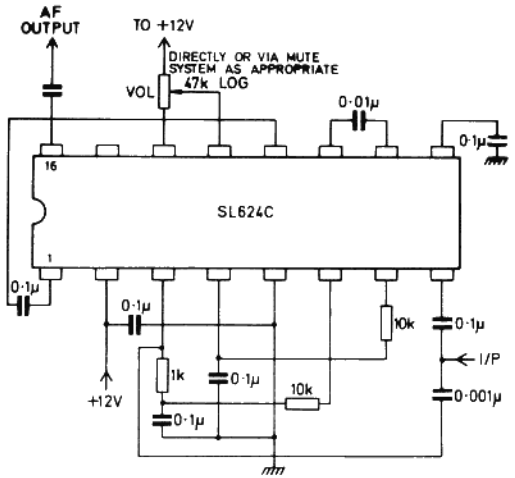


Fig. 20 AM detector

AM Detector

The AM Detector illustrated in Fig. 20 is a synchronous detector i.e., the carrier is separated from the modulation by the limiting amplifier and is then mixed with the whole signal in the modulator to give a demodulated audio output. Such a system has a great advantage in modern receivers (where a single block filter precedes a high gain broadband IF amplifier) in that nearly all noise products (produced by the modulator

mixing the incoming carrier with broadband noise from the IF amplifier) are out of the audio range and are therefore, not available. With an envelope detector – such as a diode – all this noise is detected, much of it within the audio passband, and the detector performance is degraded.

A disadvantage of the system, however, is that if the level of the input signal is so low that the limiting amplifier fails to limit during modulation troughs severe distortion occurs, and if there is no input signal there is a large noise output. Adequate squelch is therefore necessary. Again, this may be derived from the limiting amplifier by the circuit Fig. 19.

To ensure that sufficient signal is applied to the limiting amplifier the input signal amplitude should be at least 2mV r.m.s. Even then some difficulty may be experienced with signals having over 97% modulation – but such signals are not usual. An input signal of 5mV is a good target value but the detector will handle signals up to 50mV without difficulty. To keep the input within this range AGC is required. In a speech system an audio AGC system such as the SL 621C (its sensitivity modified by a series input resistance) is ideal. Its only drawback is that if an unmodulated carrier is received no AGC is produced and the amplifiers in the system can overload. Therefore the better system to use is that shown in Fig. 21. In this circuit an SL621 normally controls the system to hold

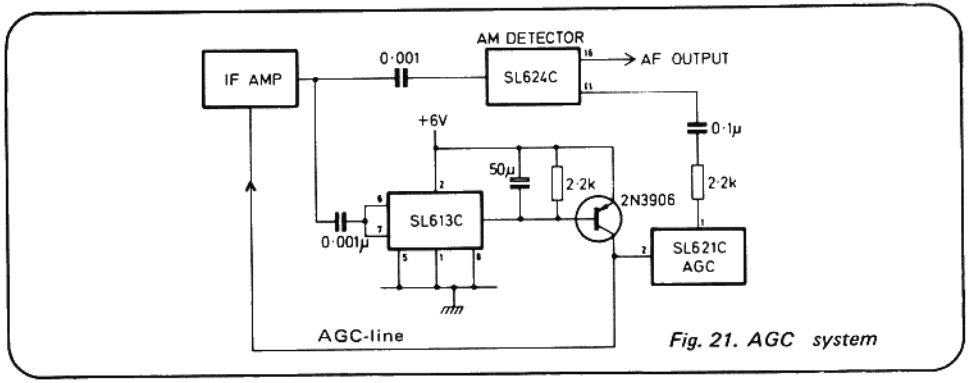


Fig. 21. AGC system

the audio output constant, and if an unmodulated carrier is received the extra RF detector provides sufficient AGC to prevent the IF amplifier from saturating. A big advantage of this system over the simple carrier AGC used in most AM receivers is that the audio output does not vary with modulation depth – thus, the volume control need rarely be adjusted.

SSB Detector

In the SSB detector of Fig. 22 the limiting amplifier is connected as a BFO and the signal input is applied to the modulator input. The system is similar to the AM system above except that the carrier is generated by an oscillator rather than recovered from the signal. The input signal requirement is again 50mV maximum but in this case inputs lower than 5mV can be tolerated if the resulting lower output is acceptable. Carrier squelch is not possible – if squelch is required it must be derived from the SL621C AGC system, but since the BFO runs continuously detected noise is less of a problem and squelch is not really necessary.

AM/SSB Detector

This detector consists of an AM detector as described above, with a separate input on pin 4. During AM reception this input is not driven, but during SSB reception it is driven with a 200mV signal from a separate BFO. This swamps the input on pin 3 and the device acts as a product detector.

It is possible to make the internal limiting amplifier function as a switched limiting amplifier/BFO but this presents layout difficulties. It is much easier to use an extra transistor as a BFO.

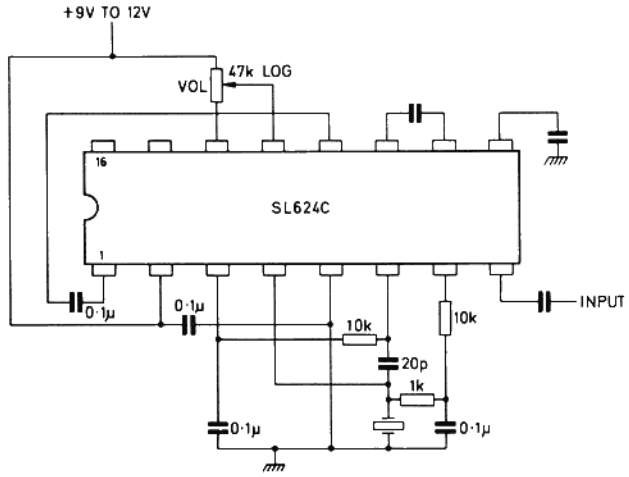


Fig. 22 SSB detector — self- oscillating

Microphone/Headphone Amplifier SL630C

The SL630C is an audio amplifier having 40dB gain and an internal gain control of approximately 60dB, and an output capability of 200mW into a 40Ω load when used with a 12V supply. The SL630C is designed for use with the SL620 AGC generator.

CIRCUIT DESCRIPTION AND APPLICATIONS

To maintain HF stability — particularly on negative half-cycles — the output (pin 1) should be decoupled by a 1,000pF, low series inductance, capacitor placed directly between pins 1 and 10 with leads cut as short as possible. This component must be on the integrated circuit side of the output coupling capacitor. At high supply voltages and/or low temperatures 10Ω must be placed in series with this capacitor and 100pF connected from pin 4 to earth. The output is coupled to its load with a capacitor of a low impedance relative to the load at the lowest frequency to be used. The load may be resistive or reactive and, for maximum power output, should lie on the load/supply voltage line (see Technical Data). *Any higher value of load impedance is quite safe but the device will over-dissipate and eventually destroy itself by overheating if the output is short-circuited.* The optimum load therefore, at any rate with supplies of over 9V, can be regarded as a safe minimum. The circuit shown in Fig. 23 which shows the SL630C used as a headphone amplifier, may also be used with loudspeakers having suitable impedances. The distortion is about 0.5% at full output.

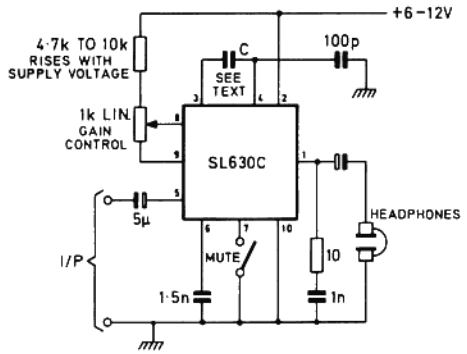


Fig. 23 Headphone amplifier using the SL630C.

The power supply, to pin 2, should be between +6V and +12V and adequately decoupled both at HF and LF. The quiescent power consumption at various supply voltages is shown in the Power characteristics, as is the relation of the supply voltage to the optimum load and the maximum power available (see Technical Data).

A capacitor connected to pins 3 and 4 defines the high frequency response of the amplifier. The upper 3dB frequency, f, is given by the formula:

$$f = \frac{16000}{C + 20} \text{ kHz. (C is in picofarads)}$$

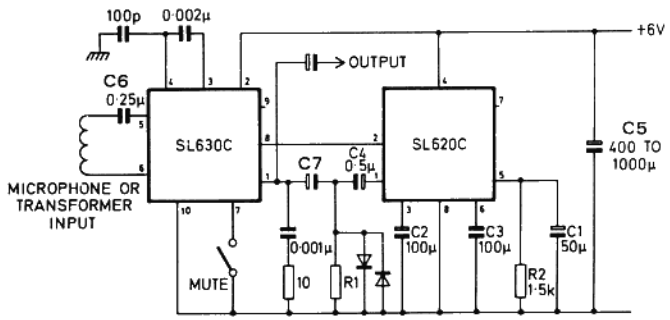


Fig. 24 Audio amplifier with AGC.

Pins 5 and 6 are input terminals. They may be used together as a differential input, in which mode they present an impedance of approximately 2kΩ and result in a voltage gain (without gain control) of 100 (40dB). When the input is obtained from a magnetic transducer or a transformer it is desirable to use the differential input mode since the signal winding may be connected directly between pins 5 and 6 and no other components are required. This input is also recommended when the SL630C is being used with an SL620C in the automatic gain control system described below (Fig. 24), but in this case it is best to connect 0.25µF in series with the signal winding to minimise offset effects when AGC is applied. *Pin 6 should always be decoupled at RF by 1500pF to earth.*

An input may also be applied between pin 5 and earth. In this case the gain is 200 (46dB) and the input impedance 1kΩ. Pin 6 should be earthed by 1500pF. A coupling capacitor is required between the input and pin 5.

The circuit is muted by earthing pin 7. A muted circuit attenuates an input by about 100dB

Gain control is applied to pin 8, which has an input impedance of 3.6kΩ. It must be appreciated that even with full gain control the input cannot exceed 50mV rms without clipping so that at high control levels the output level is limited. The AGC characteristics will vary with temperature but, as shown in Fig. 23 a potentiometer to give manual gain control can be connected to the internal bias point at pin 9 which provides a temperature-compensated reference at the voltage at which gain control commences. Pin 10 is the signal earth and negative power supply connection.

The SL630C used with an SL620C in an AGC controlled circuit is shown in Fig. 24 With regard to this application, the following points should be noted:

1 The time constant R1C7 must be 800µs and R1 must not exceed 300Ω. Within these limits R1 may be the external load but if the external load impedance is likely to vary or be larger than 300Ω it should be connected directly to pin 1 via an appropriate capacitor and R1 and C7 should be separate.

2 C6, whose use is not essential, reduces the risk of motor-boating (VLF oscillation). If an electrolytic capacitor is used it may be connected with either polarity as there is only 10mV across it.

3 R2 is also non-essential but is useful if the input is likely to contain a large component below 300Hz.

4 C5 should be used if the power supply has a source impedance of more than a few ohms or is connected by long leads.

Double Balanced Modulators SL640C & SL641C

A modulator is a device the output of which is the product of its two inputs. Modulators are extensively used as frequency changers, phase detectors and in many other applications. If two frequencies, f_1 and f_2, are applied to the inputs the output consists of the frequencies $|f_1 + f_2|$ and $|f_1 - f_2|$.

Many types of modulator are known, rather fewer are in common use. The most common is probably the diode ring – this has the advantages of good signal and carrier rejection and simple structure. It also has several drawbacks: it must be set up carefully, it needs two or three tuned transformers, its gain is less than unity and it needs a high level signal to one of its inputs.

The transistor double-balanced modulator, of which the Plessey SL640C and SL641C are examples, is less well-known than the diode ring, despite several advantages. This is because, until the advent of integrated circuits, it was too complex and expensive a procedure to accomplish the matching necessary to make a double-balanced modulator with transistors. Transistors in integrated circuits, however, are intrinsically well-matched so that, if a double-balanced modulator is made as an integrated circuit, little if any external balancing is necessary. Furthermore, and in contrast to a diode ring, such a modulator needs little setting up, no transformers or tuned components, and only low-level inputs. Its gain may be greater than unity.

PRINCIPLES OF OPERATION

A simple double-balanced modulator is shown in Fig. 25. It is evident that the sum of the two output currents equals the tail current and that, from considerations of symmetry, if either V1 = V2 or V3 = V4 then I1 = I2. Also if $R \gg R_e$ the collector currents of TR1 and TR2 will differ by an amount proportional to the difference between V1 and V2. If, therefore, a small input at frequency f_1 is applied between V1 and V2 and a large signal at f_2 is applied between V3 and V4, sufficient to turn the transistors TR3, TR3', and TR4, and TR4', fully on and off, it is evident that switching modulation, similar to that of a diode ring will occur and frequencies $|f_1 \pm f_2|$ will occur at the output as will sums and differences of f_1 and the odd harmonics of f_2 i.e. $|f_1 \pm 3f_2|, |f_1 \pm 5f_2|$, etc.

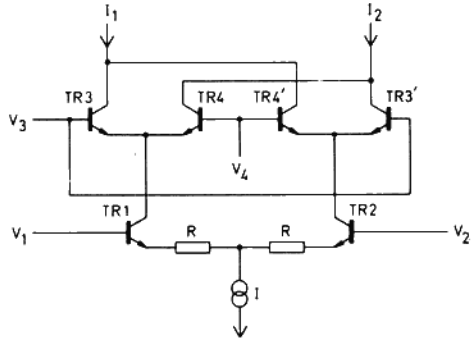


Fig. 25 A transistor double-balanced modulator.

CIRCUIT DESCRIPTION AND APPLICATIONS

The circuits of the SL640C and SL641C are very similar but have different signal input and output configurations – these are fully discussed below.

The circuits require a single, well-decoupled positive supply of between 6 and 9 volts and consume about 12mA. Pin 2, an internal bias point, must also be decoupled by a low-leakage (<100nA) capacitor having a low reactance at the lowest signal or carrier input frequency.

Pin 1, which is connected to the can, should be earthed to prevent HF pickup.

The input and carrier signals, which should not exceed 200mV rms, are applied to pins 7 and 3 respectively. Both the SL640C and the SL641C have a carrier input impedance of 1kΩ and 4pF and the SL641C has a similar signal input impedance. The signal input impedance of the SL640C is 500Ω and 5pF. The input coupling capacitors should have a leakage of less than 100nA and an impedance of less than 100Ω at the lowest frequency they will carry. This should be reduced to less than 10Ω above 10MHz.

The output of the SL641C is intended as a current drive to a tuned circuit. If both sidebands are developed across this load its dynamic impedance must be less than 800Ω; if only one sideband is significant this may be raised to 1600Ω and it may be further raised if the maximum input swing of 200mV rms is not used. The dc resistance of the load should not exceed 800Ω. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8kΩ at AC or DC. This, of course, increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350Ω and 8pF and the other is the emitter of an emitter follower connected to the first output, which requires a discrete load resistor of not less than 560Ω. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

The circuits will operate with input frequencies between 1Hz and 70MHz with the performance given in the Technical Data; the SL641C will operate at up to about 150MHz with reduced performance. To use them at frequencies below 100Hz precautions must be taken to prevent leakage in the input coupling capacitor from altering the device bias.

Some applications of the SL640C and SL641C are shown in Figs. 26 and 27. Power, decoupling, and earth connections are not shown.

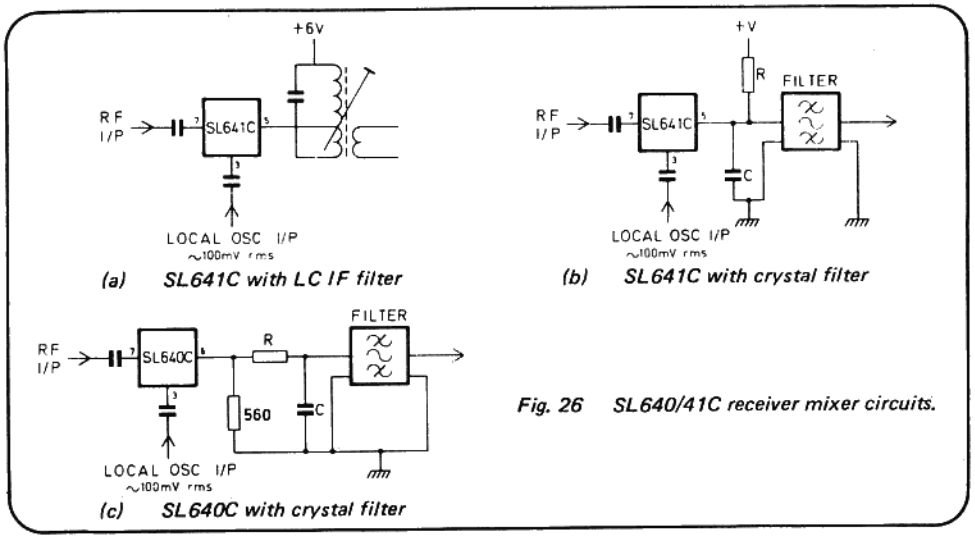


Fig. 26 SL640/41C receiver mixer circuits.

Fig. 26a shows the SL641C used as a receiver mixer driving a wound IF coil and Fig. 26b shows it driving a crystal filter. R and C must be selected to match the filter. If R is less than 800Ω it may be connected to the +6V line supplying power to the SL641C; if it is between 800Ω and 1.8kΩ it should be connected to +9V (while the SL641C supply must remain at +6V). If R is greater than 1.8kΩ the circuit in Fig. 26b is unsuitable and the SL640C circuit illustrated in Fig. 26c should be used.

The SL640C and SL641C have a noise figure of about 10dB at 100Ω source impedance. When used as receiver mixers they have better than −40dB intermodulation products so long as unwanted signals do not exceed 30mV r.m.s. Thus, either can be used as a receiver mixer at HF without an RF amplifier since atmospheric noise will far exceed device noise at these frequencies if the antenna is reasonably good. If an SL610C RF amplifier is used the intermodulation threshold will be reduced to 3mV r.m.s. (since the SL610C has a gain of 10). The SL640/41 is then less attractive as a mixer and a diode ring mixer should be used.

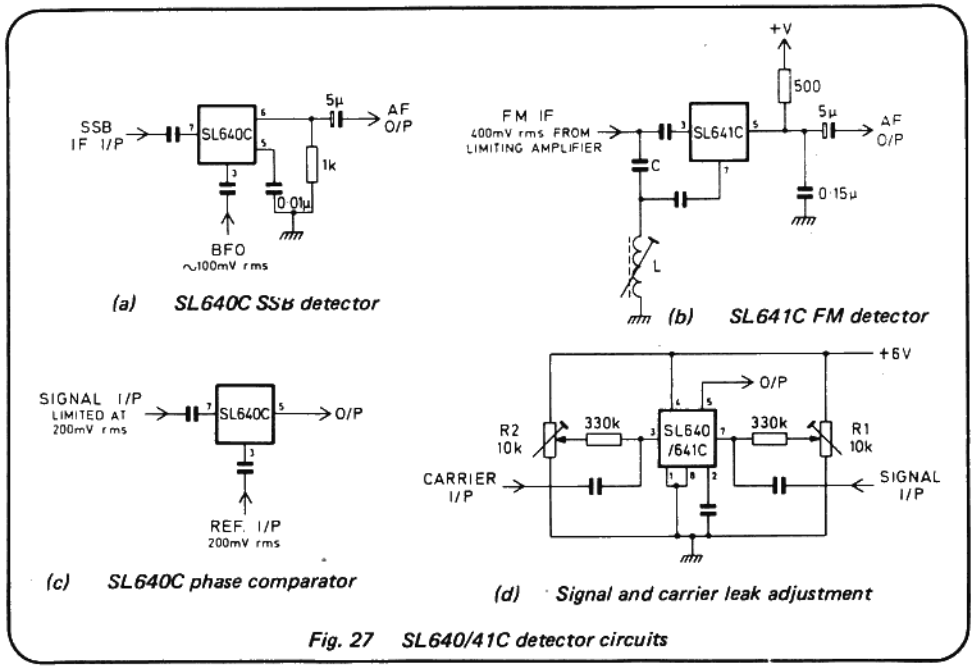


Fig. 27 SL640/41C detector circuits

Fig. 27a shows the SL640C used as an SSB detector. The capacitor connected to output pin 5 decouples the sum frequency $|f_1 + f_2|$, while the audio difference frequency $|f_1 - f_2|$ is taken from pin 6. An FM detector is shown in Fig. 27b but the function is better performed by a Plessey Semiconductors SL624C integrated circuit, which has its own limiting amplifier. The phase comparator shown in Fig. 27c is more useful – it may be used as a detector for phase modulated signals or as a comparator in phase-locking systems such as frequency synthesisers.

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig. 27d. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

Fig. 28a shows the SL640C or SL641C used as a sideband generator. Both sidebands are produced so that if a single sideband is required it must be obtained by subsequent filtering (Fig. 28b). If pin 2 is earthed by a resistor of about 15kΩ (its actual value may

need to be selected) the device's carrier leak is increased to a point where the DSB signal becomes AM. This is useful where it is desired to select sideband or AM. In the circuit shown in Fig. 28c a single sideband only is produced. It is important that both the audio and carrier reference and quadrature signals should be accurately 90° out of phase. The amplitude of one phase of audio should be adjusted to obtain maximum second sideband rejection.

If the carrier reference is connected to input A, and the carrier quadrature to input B, LSB output results. If the carrier quadrature is connected to input A, and reference to input B, USB output results.

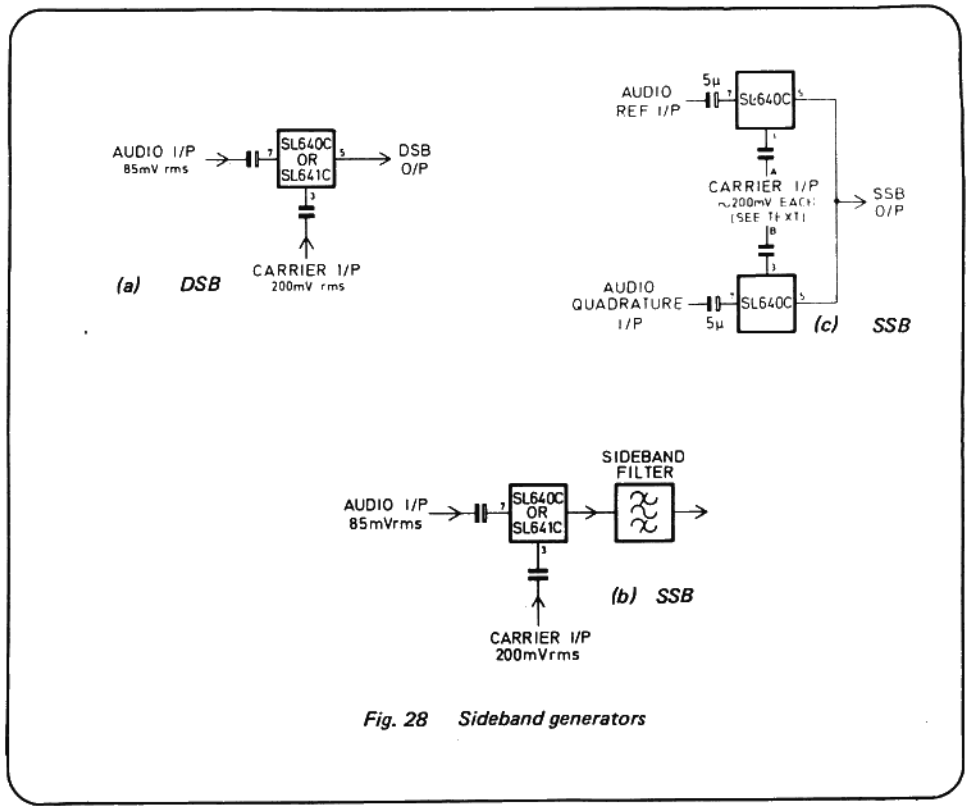


Fig. 28 Sideband generators

Frequency multiplier and divider circuits are shown in Figs. 29 and 30. This particular application of double-balanced modulators is not practicable with diode ring modulators where high carrier powers are required but only low power outputs are produced. The circuits shown are examples – many other more complex configurations are possible. It is advisable to tune the outputs to remove unwanted sidebands.

Many other applications of the SL640C and the SL641C are possible, such as speech scramblers, and electronic music generators. The devices may, in fact, be used wherever multiplication, phase sensitive detection or frequency changing are required.

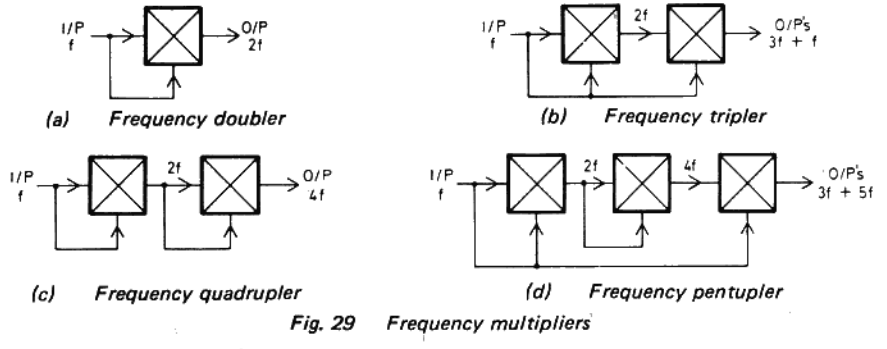


Fig. 29 Frequency multipliers

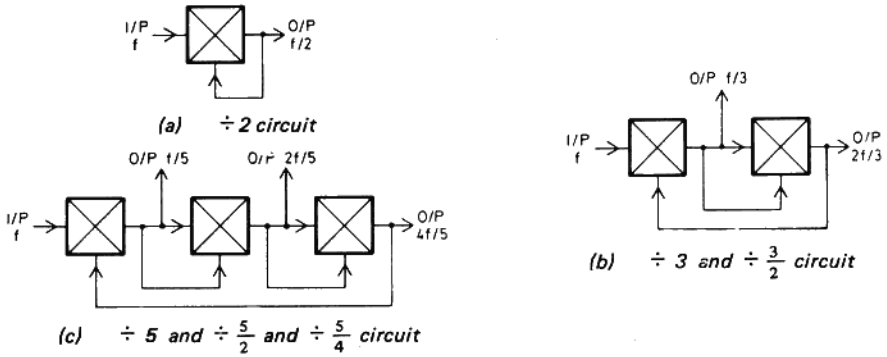


Fig. 30 Frequency dividers.

The final outputs should be tuned so that harmonics are not fed back.

Square Law Device SL645C

The SL645C is a two-quadrant square law device. It is intended for use as a frequency doubler or as a true r.m.s. detector.

CIRCUIT DESCRIPTION

The circuit diagram of the SL645C is shown in Fig. 31. In normal use it is connected as in Fig. 32 and an input applied either as an unbalanced input to pin 2 or pin 7 (the unused pin being earthed via 50 ohms), or as a balanced input to both pin 2 and pin 7. Two outputs are available – on pin 4 an output at double the input frequency and on pin 5 a current proportional to the square of the input voltage. In fact both outputs are available on each pin but pin 4 has a lower self-capacitance and a large standing current, making it more suitable for AC outputs, whereas pin 5 has a low leakage current making DC measurements simpler. The circuit will accept inputs at frequencies up to 200MHz with amplitudes up to 600mV p-p.

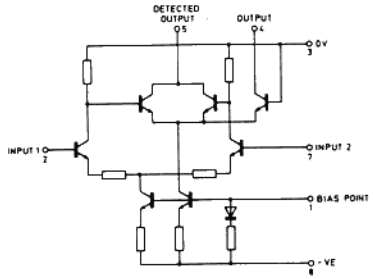


Fig. 31 Circuit diagram of the SL645C

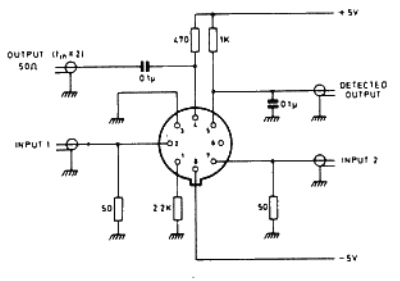


Fig. 32 SL645C application

The tail current in the two long-tailed pairs is set by feeding a current into pin 1. Normally this is achieved by connecting a resistor of about 2.2kΩ between pins 1 and 3. If the circuit is being used as a frequency doubler the fundamental rejection may be optimised by slight adjustment of this resistor. There should be a low DC resistance between the input pins 2 and 7, and between each of these pins and pin 3 but, since they have an input impedance of about 10kΩ in parallel with 1pF, they may be fed with quite high impedance sources (e.g. tuned circuits). Input signals may be applied to both inputs in antiphase or to one only, the other then being earthed to pin 3.

The SL645C requires both a positive and a negative supply. The negative supply (pin 8) must be well decoupled and should be usually between –5V and –6V. The centre rail is pin 3 and the positive supply is connected to pins 4 and 5 via load resistors or tuned circuits, or directly to an unused output. The positive supply is usually of the same magnitude as the negative supply, but may be up to +9V. The maximum current in pin 4 or 5 is about 300μA and the load resistance must be such as to keep these pins more positive than pin 3 at all times.

Pin 5 has a standing current of about 50μA, increasing with the square of the input voltage; at 600mV p-p input it is about 250μA. Pin 5 is normally used for square law detection, the output being taken as a current, or as a voltage across a load resistor connected to the positive supply.

Pin 4 has a low capitance (0.5pF) and a standing current of about 250μA. The output, at twice the input frequency, is usually taken from this pin as either a current, or as a voltage developed across a load resistor or tuned circuit. With 600mV p-p input the output at 2f is a current of 200μA p-p. The conversion voltage gain is therefore Z/3 where Z is the load impedance in kilohms. Hence in a 50Ω system the frequency-doubling conversion loss is approximately 35dB. Fortunately, in systems of cascaded SL645Cs, tuned loads (with high resonant impedances) are possible, avoiding the necessity for interstage amplifiers.

A typical frequency multiplier chain is shown in Fig. 33.

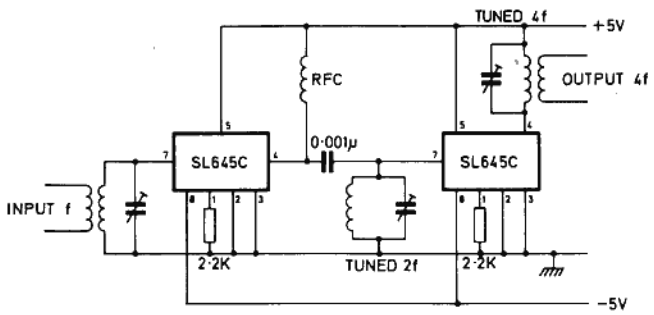


Fig. 33 Frequency multiplier chain using SL645Cs.

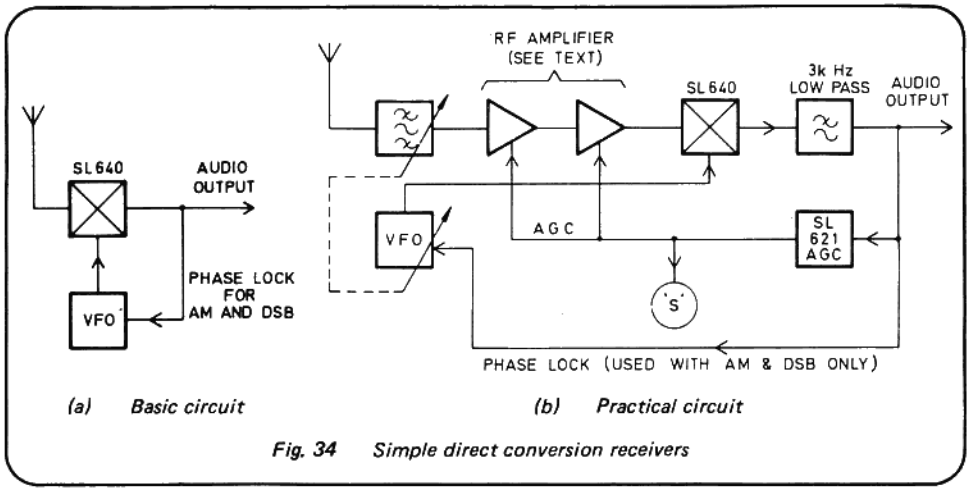
System Design 2

Receiver Systems

THE SYNCHRODYNE

The simplest receiver that can be built from SL600 devices is the Synchrodyne, an example of which is shown in Fig. 34a. Such direct conversion receivers may be used for the demodulation of SSB, AM and DSB, where the VFO is tuned to the carrier frequency (for AM and DSB the VFO must be phase-locked to the carrier). For CW reception, the VFO is tuned a few hundred Hertz away from the carrier, resulting in an audible beat with the CW. Upper and lower sidebands are equally well detected by this receiver, which can be very selective if the audio passband is limited. If, however, a Synchrodyne is used to receive, say, an upper sideband SSB signal with a carrier frequency f kHz, then another such signal with carrier frequency lying between f and (f – 3) kHz will, if present, be detected (though not intelligibly) and cause interference. The interference can be removed, and one sideband only detected, by use of the phasing system shown in Fig. 35

The system in Fig. 34a is, of course, only a detector; as such it is not very sensitive and has no AGC. A more complete system, illustrated in Fig. 34b, has RF filters to minimise cross-modulation, an RF amplifier (or RF amplifiers), AGC and an optional 'S' meter. Whether one or two RF amplifiers are used will depend on the sensitivity required and the AF gain available; these factors, together with considerations of operating frequency, will determine the choice of device from the SL610C, SL611C and SL612C range. The SL612C has the additional advantage of a lower current consumption and slightly lower noise figure.



(a) Basic circuit *(b) Practical circuit*

Fig. 34 Simple direct conversion receivers

Fig. 35 shows a more complex direct conversion receiver which employs RF and AF phasing to cancel one sideband so that it is a truly single sideband receiver. It is necessary to have accurate phasing of the signals and well-matched gain in the two audio channels before the summing stage. Upper or lower sideband may be selected by reversing the phasing of the RF or, for simplicity, the audio signal. The system illustrated detects LSB when the upper channel is in phase, USB when it is out of phase by –90°.

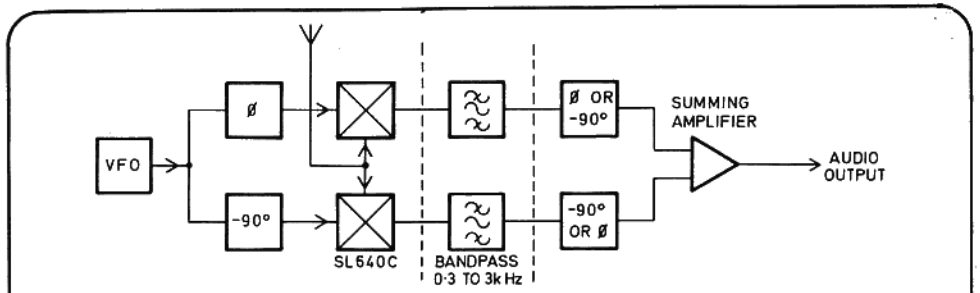


Fig. 35 SSB direct conversion receiver

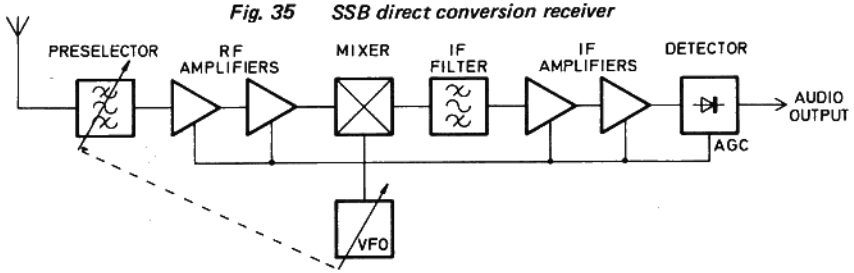


Fig. 36 The traditional basic superhet

THE CONVENTIONAL SUPERHET

A basic superhet is shown in Fig. 36. The signal from the antenna, having passed through a preselector filter, is amplified and then mixed with a local oscillator to produce an intermediate frequency. This IF signal is filtered to remove signals on adjacent channels, amplified and applied to a detector. An AGC voltage is fed back to the RF and IF amplifiers.

This system has been in use, first with valves and distributed IF amplifiers – later with transistors and/or block crystal filters – since the late 1920s. In many respects it is ideal – it has high gain, low noise and excellent selectivity. Many of the most famous receivers of the past used such a system but it has one severe drawback – the large gain in the relatively broadband stages prior to the IF filter can lead to large unwanted signals being applied to the mixer which in turn (and especially with transistor mixers) leads to cross-modulation. Once cross-modulation has occurred no amount of subsequent filtering will cure it. The problem was less severe in the past for two reasons – the valve mixer is far less susceptible to such effects, and, far more important, in the past there were far fewer strong signals liable to cause such troubles than there are on today's crowded frequencies.

Modern receiver design has moved away from such techniques. The design of HF and VHF receiver front ends is a difficult task and the systems used in the highest performance receivers are often not only complex but closely guarded secrets as well. In principle, however, two criteria must be considered – firstly, a minimum of gain between the antenna and the crystal filter (usually none at HF where antenna noise levels are high but possibly 10dB at VHF and UHF so that mixer noise does not control system sensitivity; in mobile radios at VHF/UHF, however, sensitivity is often sacrificed for strong-signal performance) and, secondly, the use of a mixer having as great a cross-modulation resistance as possible. Some common mixers are discussed below.

The bipolar transistor is a very poor mixer and suffers badly from cross-modulation. Its common use in television tuners is responsible for their extreme susceptibility to cross-modulation by local transmitters. However, the use of bipolar transistors in the microwave region can give some cost advantages over other systems. Junction FETs, although far better for the purpose than bipolar transistors, do not make ideal mixers when used alone.

Cross-modulation resistance can be greatly improved by employing bipolar transistors in double-balanced modulator circuits such as the SL640 or SL641. The SL640/1 will tolerate up to 30mV r.m.s. of unwanted signal before cross-modulation of a 1μV signal reaches 1%. This is not a very good performance by the standards of modern HF receivers; nevertheless the SL640/1 may be used in medium performance receivers where its low local oscillator power requirement and extreme ease of use in some degree compensate for its less than ideal large signal performance. It should be noted that if the SL640/1 be preceded by an SL610 to which no AGC is applied the signal at the antenna needed to produce cross-modulation is reduced from 30mV to 3mV. This is not satisfactory.

A single balanced modulator using a matched pair of junction FETs can have useful gain, low noise, and high cross-modulation resistance, but has one disadvantage in that quite high local oscillator power is required. Nevertheless, it has been demonstrated that a mixer with 2.5dB gain, working from 50MHz to 300MHz and capable of handling signals in excess of 2V r.m.s. can be made using this technique.

The dual-gate MOSFET is another useful mixer. The fact that it is more often used at VHF than at HF appears to result more from custom than for any real technical reason. It will handle signals of over 150mV but its biasing is somewhat critical. Local oscillator requirements, however, are modest and it can have both useful gain and low noise figure.

Of all the mixers in use today, however, the diode ring is undoubtedly the best. Using four matched diodes of any type (most commonly used are silicon Schottky diodes and, in low-cost systems, germanium diodes), this mixer has many advantages. It is bi-directional (so that it may be permanently connected to the filter of any transceiver and yet be used on both transmit and receive (see Fig. 45), it will suppress very large unwanted signals – although this is also dependent on the local oscillator power inserted – and can be used at frequencies up to several GHz. Disadvantages of the diode ring mixer are its high local oscillator requirement, its conversion loss of about 6dB and its noise figure of 5dB or more. Several manufacturers make silicon Schottky diode rings with very broadband 50Ω ports at quite reasonable prices. These are used wherever diode ring mixers are specified in this application note.

The mixer, therefore, and any RF amplification preceding it, must be as resistant as

possible to cross-modulation. It may be noted that while an SL640/1 can only tolerate 30mV r.m.s. of unwanted signal, an SL610 without AGC will accept 100mV – but a mixer capable of handling 1V would have to follow it. Using an SL610 with full AGC cross-modulation is encountered at about 250mV r.m.s. input. The mixer must be followed at once by the filter. In modern sets a crystal or ceramic filter is usually employed, so no other type will be considered here. The bandwidth of the filter depends on the signal being received – bandwidths commonly used are given in Table 2.

Signal Mode	BW (kHz)
CW (morse code)	0.3 – 0.6
SSB	2.7
AM (Voice)	5.5
NBFM	10 – 25 (Usually 12)*

* This depends on how NB the FM is

Table 2

The filter is followed by a high gain broadband IF amplifier consisting of two or three SL612s followed in turn by a detector, AGC generator and the audio stages.

AN SSB RECEIVER

A receiver as outlined above is described in detail in Appendix B as the receiver section of an SSB transceiver. Its circuit diagram is given in Fig. 37. It consists of a diode ring mixer fed from the antenna via a preselector followed by a crystal filter (an SEI QC1246 AX 2.4kHz bandwidth 9MHz filter was used in the prototype) and a 3-stage SL612C IF amplifier. An SL640C acts as product detector and feeds an SL621C AGC generator and an SL630 audio amplifier.

The AGC line is decoupled to keep RF from the AGC inputs of the SL612Cs but too large a value of decoupling capacitor degrades the impulse interference suppression characteristics of the SL621C. This type of suppression, while not as effective as a full noise-blanking circuit, nevertheless reduces impulse interference to an acceptably low level for most receivers. A suitable total capacitance on the AGC line is 0.015μF. The resistor in the AGC line of the first SL612C should be larger than the resistors in the AGC lines of the other two devices; alternatively a silicon diode could replace the resistor. Either of these techniques will ensure that the first SL612C remains at full gain for a while after the detector output has passed the AGC threshold, thus maintaining a high signal-to-noise ratio.

The supply line is decoupled at LF to prevent supply current surges (which in the SL621C can be induced by step signals) from interfering with other circuits. HF decoupling is unnecessary since the SL612Cs have sufficient internal decoupling, but it is advisable to earth the cans to pin 8. The interstage IF coupling capacitors should be kept as small as possible – at 9MHz 100pF is adequate – to ensure that LF signals at the output of one SL612C (due to noise or AGC action) do not reach the next stage and give

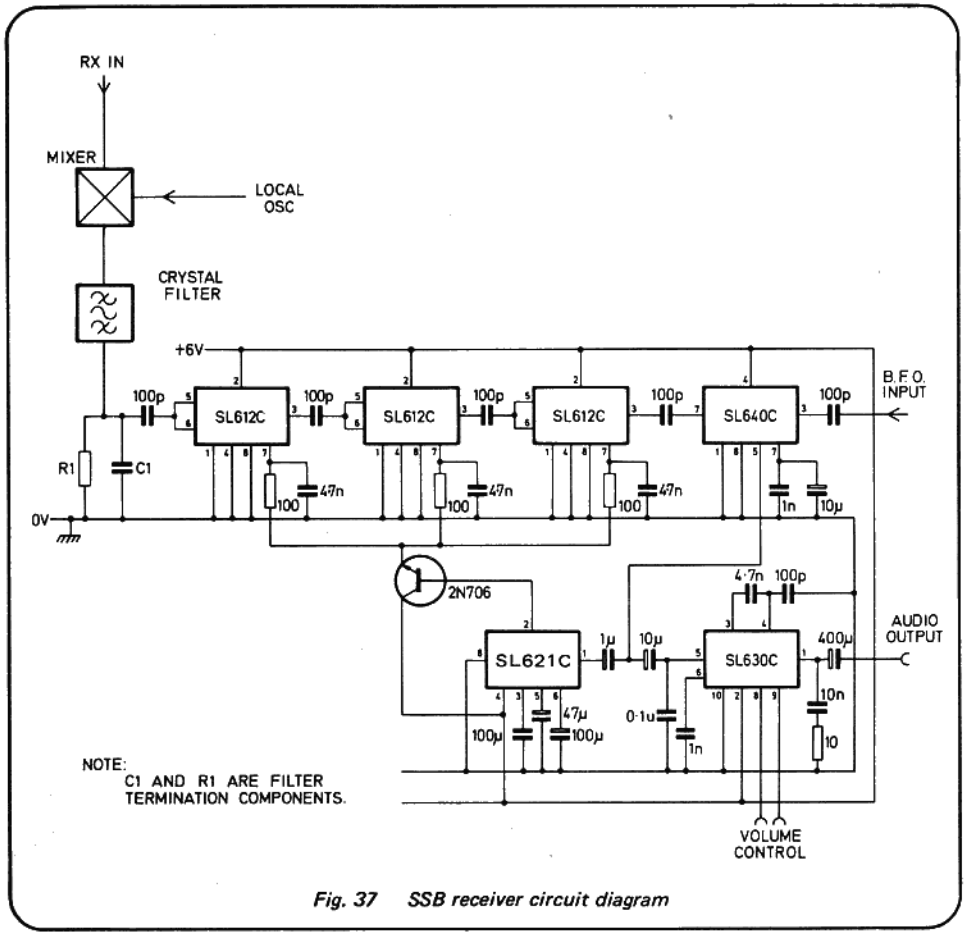


Fig. 37 SSB receiver circuit diagram

rise to low frequency instability as the receiver passes the AGC threshold.

Earlier designs of SL600 SSB receivers using SL600 devices had a preset control to adjust the AGC threshold. This is now considered unnecessary, provided that AGC to the first gain stage is delayed (as described above) until the input reaches at least 3µV. The audio output from the receiver is a maximum of 100mW which, while entirely adequate for headphone and normal domestic or fixed amateur use, may be insufficient for mobile or professional applications (although a listening test is worthwhile here, as 100mW is louder than most people imagine). If more output is needed, however, an extra power amplifier may be mounted off the board.

The circuit board described in Appendix B uses single-sided copper board. The layout is extremely critical and deviations from it are likely to lead to instability. If a different layout is used it would be better to use double-sided board and make all earth connections to a continuous unetched earth plane on the component side of the board. If

a new or different design is attempted on single-sided board, strict attention must be paid to the instructions on earth connection given in the SL610/11/12 circuit data on page 3.

MULTIMODE RECEIVERS

Front end and IF strip design in multimode receivers is identical to that described above. Differences arise in filter bandwidths, AGC and squelch systems, and detectors.

As mentioned earlier a different filter bandwidth is required for each of the four modes: CW, SSB, AM and NBFM. In the ideal multimode receiver four different filters would have to be switched, therefore, between the mixer and the IF amplifier. Since this is obviously not practical, two solutions to the problem are normally used — compromise on filter bandwidth, and cascaded filters.

The compromise technique means, in effect, that an SSB filter is used for CW SSB and AM (effectively turning AM into SSB plus carrier) while using a separate filter for FM (although the FM filter could be used for AM and would be useful if an AM signal had an FM component). The disadvantage of the compromise is that the two filters must still be switched. The stopband attenuation of modern crystal filters is better than 90dB but the presence of switches and relays at their input and output can easily reduce this by 30dB or more simply by virtue of the additional capacitance imposed. Such a serious shortcoming, even though it can be minimised, makes cascaded filters an attractive alternative method.

The filter following the mixer in a cascaded filter transceiver has a bandwidth of 12kHz. This filter is followed by two IF stages and the signal path then splits. The FM signals are then demodulated, while AM, CW and SSB signals pass through a 2.4kHz filter and another stage of IF gain before going to the AM/SSB detector. The disadvantage is that if a weak AM, CW or SSB signal has a strong unwanted signal in the 12kHz passband, intermodulation can occur in the IF amplifier. There is no cure for this but fortunately the situation is not a common one. Fig. 38 is a block diagram of the multimode receiver section of the transceiver described in Appendix D, using these techniques. The receiver has a sensitivity of about 0.2µV at the filter input for 10dB S/N on CW and SSB and slightly lower sensitivities for AM and FM. A detailed circuit is shown in Fig. 39.

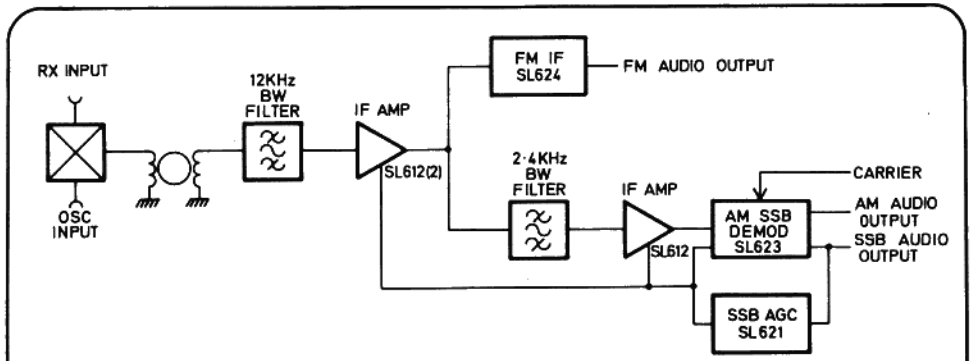


Fig. 38 AM/SSB receiver block diagram

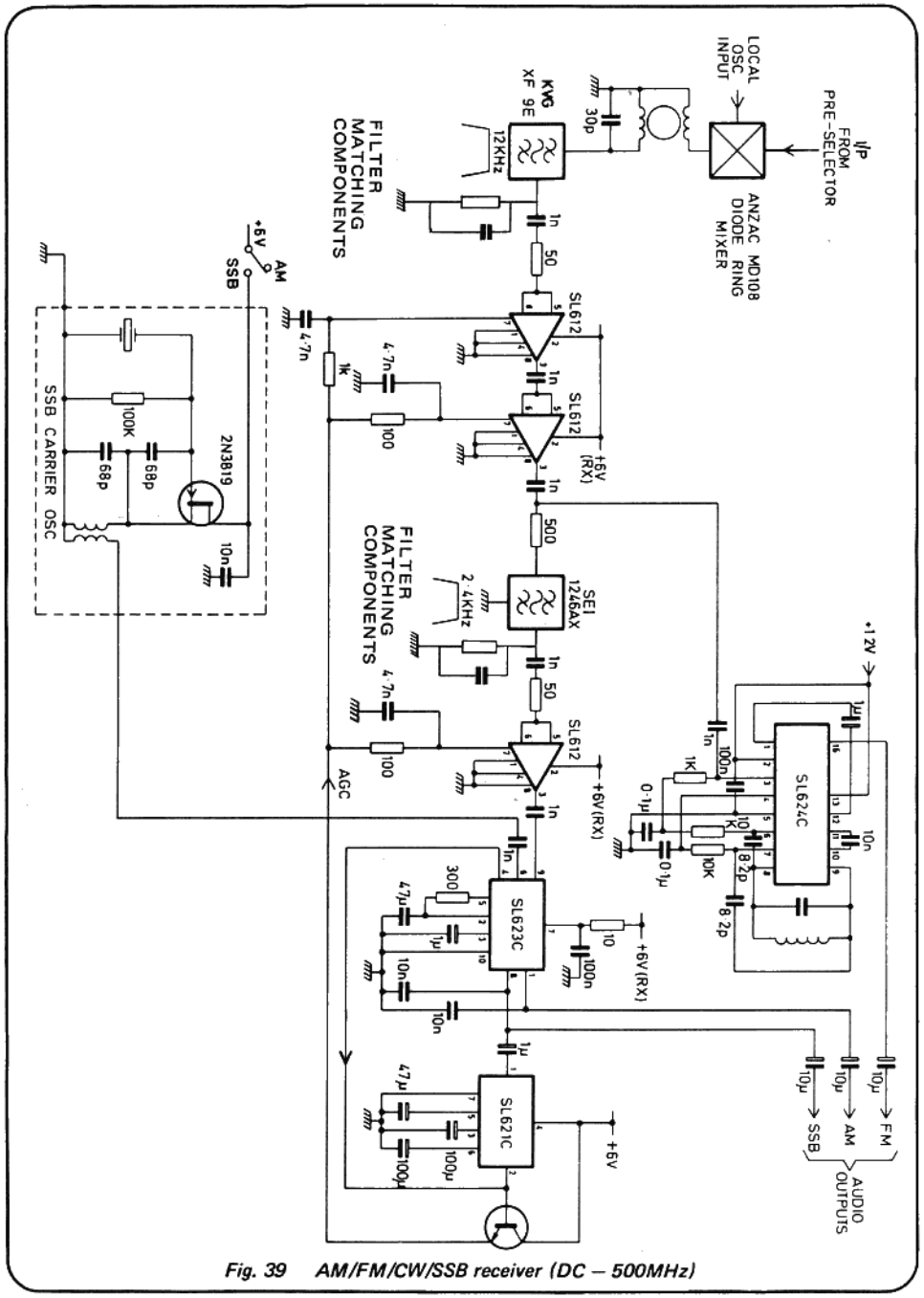


Fig. 39 AM/FM/CW/SSB receiver (DC – 500MHz)

There is little that is novel in this receiver. The input filter, a KVG XF9-E, feeds two cascaded SL612Cs which both have AGC, the input AGC being delayed. The second SL612C drives an SL624C used as an FM detector and an SEI QC1246 AX sideband filter followed by another SL612C and an SL623C AM/SSB detector and carrier AGC circuit.

The SSB output of the SL623C drives an SL621C speech AGC circuit, but only when the BFO is on. Otherwise the carrier-derived AGC from the SL623C controls the circuit. Earlier published circuits recommended that if the SL623C is preceded by three SL612Cs then a filter should be used to prevent the diode detector in the SL623C being swamped by broadband noise from the IF amplifier. The QC1246 AX performs this function, but if the circuit is copied as an AM/SSB receiver with the QC1246 AX in the front a simple filter should be retained, either between the second and third SL612C or between the third SL612C and the SL623C.

Using an SL624C in place of the SL623C however, makes such filtering and, in most cases, the third SL612C, unnecessary. This is because the SL624C demodulates AM as a synchronous detector and out-of-band noise is inaudible.

DOUBLE SUPERHETS

Double superhets can also be designed using SL600 devices but with modern filters such added complexity is rarely necessary except at UHF or where complex tuning systems are used. Inasmuch as the same techniques are used as in single superhets such systems are not described here, but it should be noted that SL600 devices have high gains, therefore too many amplifying stages should be avoided.

Transmitter Systems

FILTER TYPE SSB EXCITERS

Two types of SSB generator are in common use: filter systems and phasing systems. A basic filter system is shown in Fig. 40. The audio and a low radio frequency from an oscillator (the BFO if the system is part of a transceiver) are mixed in an SL640C which, as a result of its good carrier rejection, gives as its output a clean DSB suppressed-carrier signal. This is passed through a narrow bandpass filter to remove one sideband, the remaining sideband is converted to the final frequency by another SL640C and the image is removed by a filter. The output is then applied to the transmitter linear amplifier, possibly using a Plessey Semiconductors SL1030 as its first stage.

Fig. 41 shows a more complete filter system. It has an internal amplifier which is controlled by an automatic level control signal which, in most cases, would be derived from the final linear amplifier – either by a threshold detection system or by grid current detection in the output valve.

RF CLIPPING

The envelope of an SSB signal does not resemble the audio producing it. Therefore audio limiting and clipping are not useful techniques for increasing the average to peak

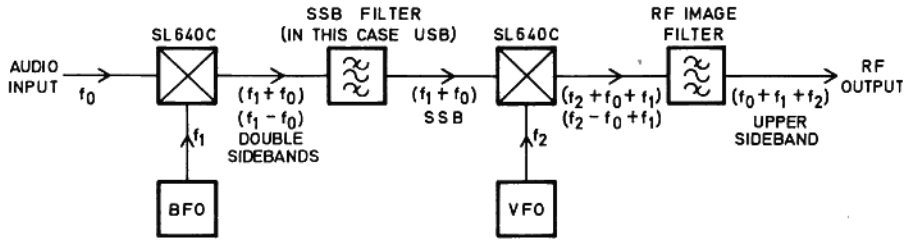


Fig. 40 Basic filter-type SSB transmitter

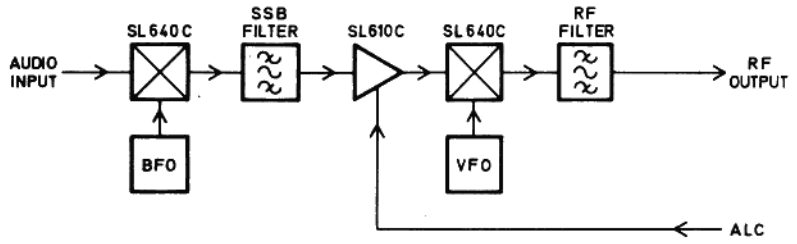


Fig. 41 SSB transmitter with ALC

power ratio of an SSB transmitter, although audio AGC, derived perhaps from an SL622C, is. Clipping must be applied to the sideband signal itself in the transmitter and the sideband must be filtered to remove intermodulation products. Such a system needs careful initial adjustment but yields good results. A typical system is illustrated in Fig. 42.

The audio input – which should be controlled by AGC – is converted to SSB as in the basic system and is then clipped by a symmetrical peak clipper, such as an SL613 or a pair of diodes. The signal is then passed through another sideband filter (to remove harmonics and intermodulation products), through an automatic level control (ALC) amplifier and, finally, is converted to the transmitted frequency. The input audio level (or the clipping level) must be adjusted so that the received audio is of adequate quality.

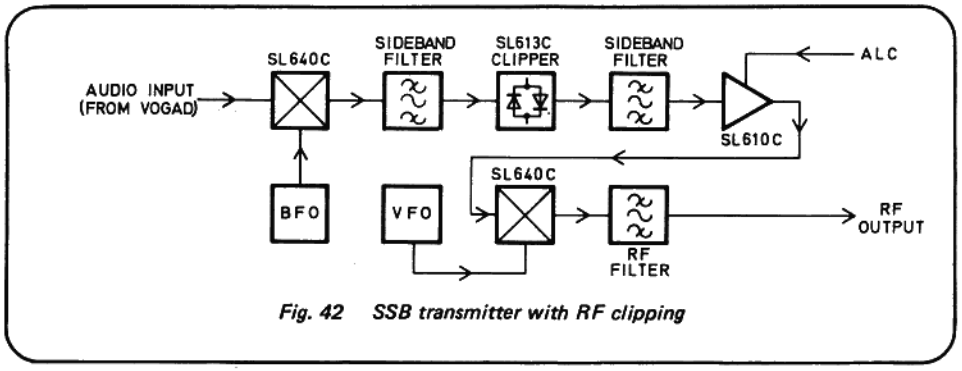


Fig. 42 SSB transmitter with RF clipping

SSB PHASING EXCITERS

A phasing system is shown in Fig. 43. The audio input, which must normally be of limited bandwidth, is phase shifted so that two audio lines of equal amplitude but separated in phase by 90° are obtained. These audio signals are applied to the signal inputs of two SL640Cs. RF reference and quadrature signals are applied to the carrier inputs, and the two outputs are summed. If the audio reference and carrier reference signals are applied to one modulator and the audio and carrier quadrature signals to the second, the LSB outputs will be in phase and will add, and the USB outputs will be out of phase and will cancel. Thus, LSB is obtained. Similarly if audio reference and carrier quadrature are applied to one modulator and audio quadrature and carrier reference to the other, USB is obtained.

This method appears attractive in many respects and has the advantages that no expensive filters are used and that the carrier frequency may be varied so that further conversion may not be necessary. It is compatible with the direct conversion SSB receiver illustrated in Fig. 35 and a very simple transceiver can be built using the two systems. The disadvantage is that to keep the second sideband the required 40dB below the desired sideband the phasing, both audio and RF, must be very accurate – in fact within 2°. In addition, the amplitude of the carrier applied to one modulator must be critically adjusted to minimise second sideband generation, and carrier leak must be minimised on both modulators.

Despite the adjustment problems, this method of SSB generation is very popular – probably because of the saving of expensive filters.

AMPLITUDE MODULATION

Amplitude modulation can be regarded as DSB with unsuppressed carrier. An SL640C can therefore be used as an amplitude modulator if its carrier leak is increased. If a 15kΩ resistor is connected between pin 2 of an SL640C and earth (as in Fig. 44) there will be sufficient carrier leak for the output of the SL640C to be AM. A simple method of selecting either AM or DSB can be implemented by switching the resistor in or out of circuit as required. If the filters following the SL640C are also switched, AM, DSB or SSB may be obtained from one SL640C with the same inputs. A multimode transmitter can therefore be made with very few components.

SCREENING

As transmitters often contain large RF fields, particular attention must be paid to screening and decoupling. In some cases it may be necessary to decouple individual stages. In areas of high field device cans should be individually earthed.

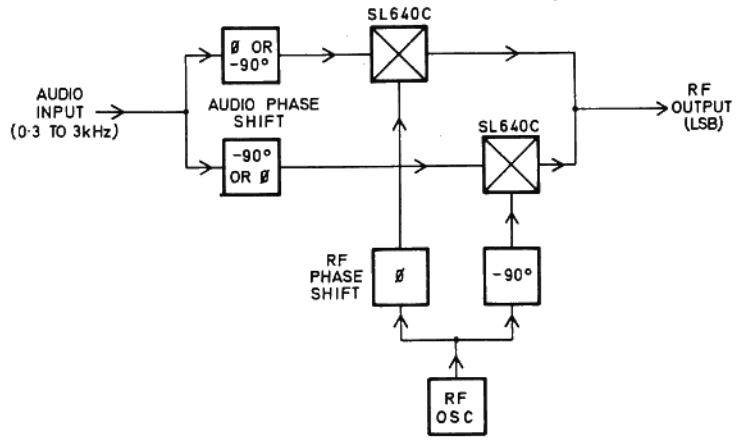


Fig. 43 Phasing exciter for SSB

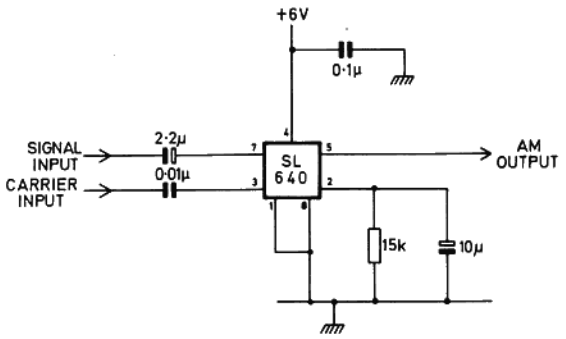


Fig. 44 Amplitude modulator

A Typical Transceiver System

SSB transmitters and receivers of the same type contain many identical components. Therefore, by a little signal switching, it is possible to make one filter perform alternately in a transmitter and in a receiver – i.e. as a transceiver. This, of course, results in a real cost saving. These points are illustrated by Fig. 45, a typical SSB transceiver, and also in Appendices B and D.

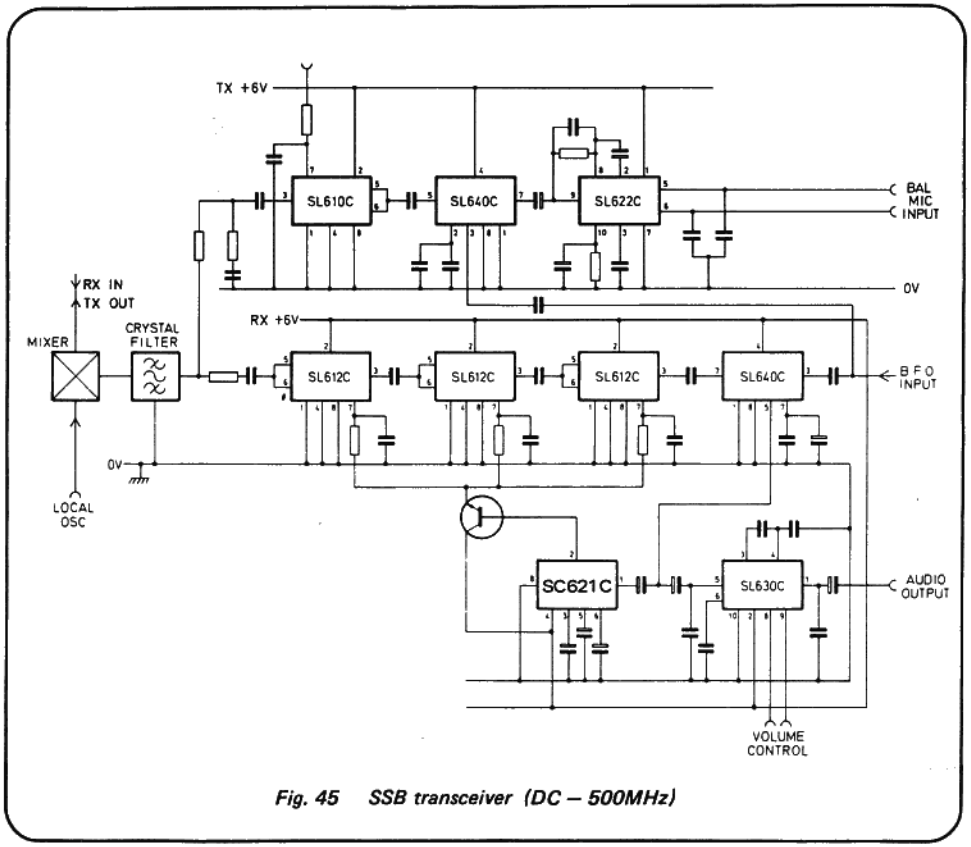


Fig. 45 SSB transceiver (DC – 500MHz)

Technical Data 3

SL610C, SL611C & SL612C

RF/IF AMPLIFIERS

The SL610C and SL611C are low noise, low distortion, RF voltage amplifiers with integral supply line decoupling and AGC facilities. The SL610C has a voltage gain of 10 and a bandwidth of 140MHz, while the SL611C has a voltage gain of 20 and a bandwidth of 100MHz. Both circuits have a 50dB AGC range with maximum signal handling of 250mV rms. As they are voltage amplifiers they have high input impedance and low output impedance.

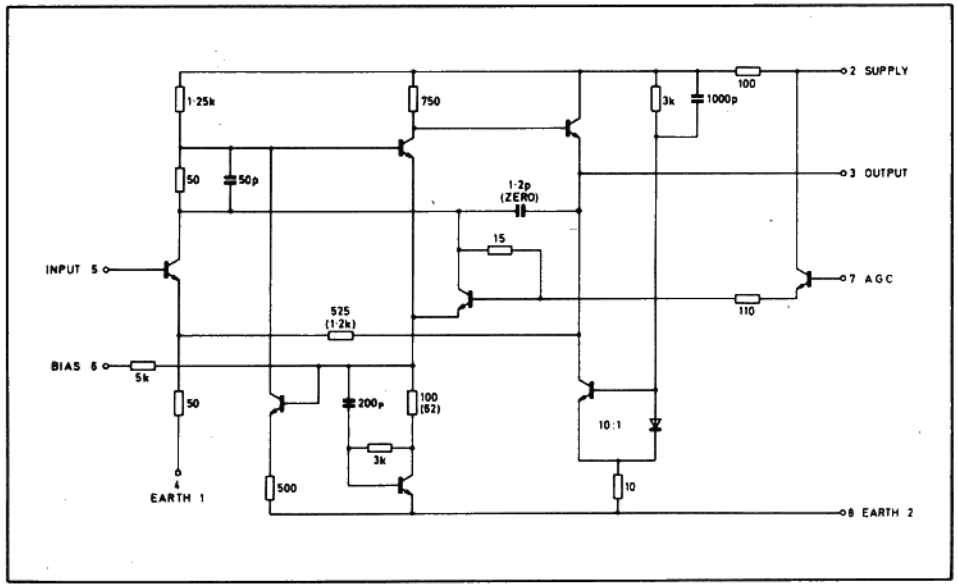


Fig. 1 Circuit diagram of SL610C and SL611C
(Component values in parentheses refer to SL611C)

The SL612C is a low noise, low distortion, IF voltage amplifier similar to the SL610C and SL611C but having a voltage gain of 50, a bandwidth of 15MHz and only 20mW power consumption. It has a 70dB AGC range with maximum signal handling of 250mV rms.

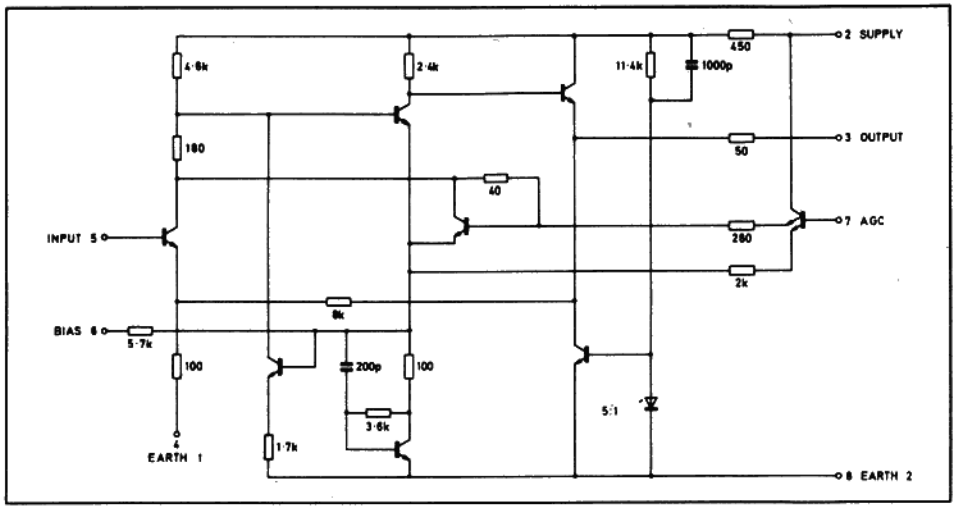


Fig. 2 Circuit diagram of SL612C

ELECTRICAL CHARACTERISTICS

Test conditions: Supply voltage = 6V
Temperature = +25°C (unless otherwise stated)
Pins 5 and 6 strapped together
AGC not applied unless specified.

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
Voltage gain	SL610C	18	20	22	dB	30MHz, Source = 25Ω
	SL611C	24	26	28	dB	30MHz, Load R ≥ 500Ω
	SL612C	32	34	36	dB	1.75MHz, Load C ≤ 5pF
Cut-off frequency (−3dB) (See Fig. 9)	SL610C	85	140		MHz	Source = 25Ω
	SL611C	50	100		MHz	Load R ≥ 500Ω
	SL612C	10	15		MHz	Load C ≤ 5pF
Noise Figure	SL610C		4		dB	Source = 300Ω, f = 30MHz
	SL611C		4		dB	Source = 300Ω, f = 30MHz
	SL612C		3		dB	Source = 800Ω, f = 1.75MHz
Max. input signal (1% cross modulation) No AGC applied	SL610C		100		mVrms	Load 150Ω, f = 10MHz
	SL611C		50		mVrms	Load 150Ω, f = 10MHz
	SL612C		20		mVrms	Load 1.2kΩ, f = 1.75MHz
Max. input signal (1% cross modulation) Full AGC applied	SL610C		250		mVrms	f = 10MHz
	SL611C		250		mVrms	f = 10MHz
	SL612C		250		mVrms	f = 1.75MHz
AGC range (See Fig. 10)	SL610C	40	50		dB	
	SL611C	40	50		dB	
	SL612C	60	70		dB	
AGC current	SL610C		0.15	0.6	mA	AGC Voltage = 5.1V
	SL611C		0.15	0.6	mA	
	SL612C		0.15	0.3	mA	
Quiescent current consumption	SL610C		15	20	mA	Output open circuit
	SL611C		15	20	mA	
	SL612C		3.3	5	mA	
Change of voltage* gain with temperature	All types		±1		dB	−55°C to +125°C
Change of AGC range* with temperature	All types		±2		dB	−55°C to +125°C

*from nominal

Gain and frequency response of these circuits are relatively independent of supply voltage within the range 6 – 9V

OPERATING NOTES

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 strapped. A slight improvement in noise figure, and an increase in the LF input impedance may be obtained by making the necessary AC connection via the earthy end of an input tuned circuit in the conventional manner.

The characteristics of these units have been expressed in G parameters which are defined as shown in Fig. 3.

These parameters correspond to the normal operation of a voltage amplifier which is usually operating into a load much higher than its output impedance and from a source much lower than its input impedance. Hence the input admittance (G_{11}) and voltage gain (G_{21}) are measured with open circuit output, and the output impedance (G_{22}) with short circuit input. The parasitic feedback parameter is the current transfer (G_{12}) i.e. the current which flows in a short circuit across the input for a given current flowing in the output circuit.

Since the effects of G_{12} are small for reasonable values of load and source impedance, the approximate equivalent circuit given in Fig. 4 may be used.

Hence the typical effects of applying finite load and source impedances, real or complex, may be evaluated by the use of the graphs showing the values of the major parameters versus frequency. At lower frequencies the limitation on Z_L is dependent upon output signal; for maximum output $Z_L = 100\Omega$.

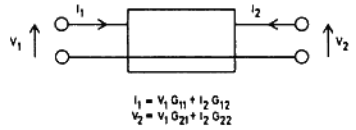


Fig. 3 Definition of G parameters

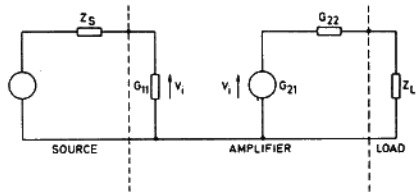


Fig. 4 Amplifier equivalent circuit

Stability

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output respectively are shown in Fig. 5 and 6 and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Fig. 7 and 8. It will be seen that, for the SL610C and the SL611C R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL612C, R_{in} is not negative and R_{out} is negative only below 700KHz.

It is evident that if an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and R1 is higher than R_{in}.

Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input may be inductive, therefore, it may be shunted by a resistor and where the load may be capacitive 47Ω should be placed in series with the output.

These devices may be used with supplies up to +9V with increased dissipation.

The AGC characteristics shown in Fig. 8 vary somewhat with temperature: a preset potentiometer should not, therefore, be used to set the gain of either of these circuits if gain stability is required.

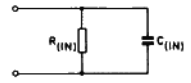


Fig. 5 Input circuit

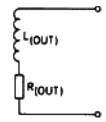


Fig. 6 Output circuit

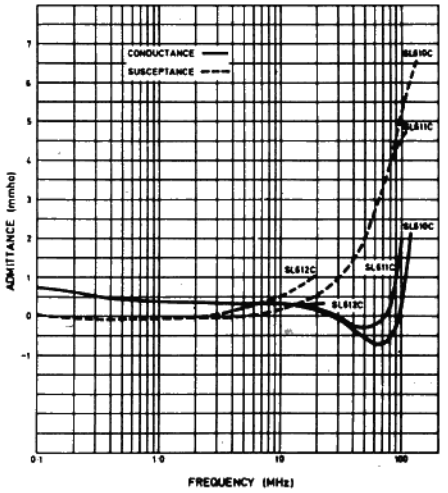


Fig. 7 Input admittance with o/c output (G_{11})

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	220°C/W
Chip-to-case thermal resistance	60°C/W
Supply voltage	12V

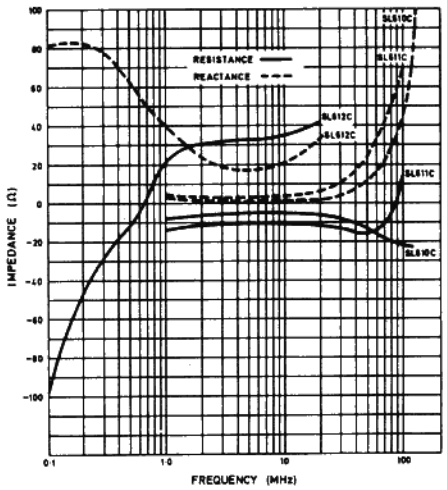


Fig. 8 Output impedance with s/c input (G_{22})

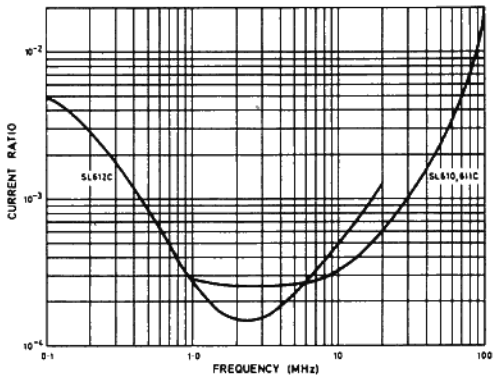


Fig. 11 Reverse current transfer ratio (G_{12})

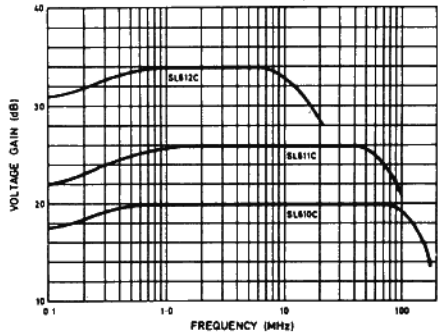


Fig. 9 Voltage gain (G_{21})

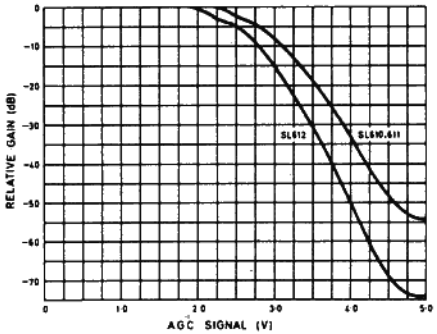
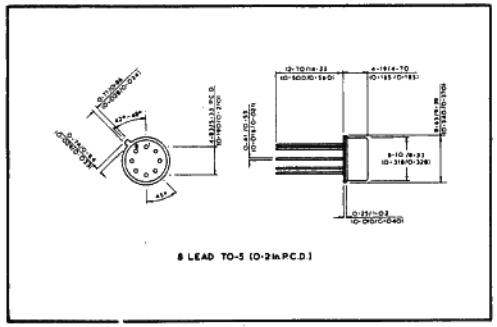


Fig. 10 AGC characteristics

PACKAGE DETAILS

Dimensions are shown thus: mm(in)



TYPICAL MAX. FREE AIR OPERATING TEMPERATURES (°C)

Supply Voltage	6V		9V		12V	
AGC Voltage	None	Full	None	Full	None	Full
SL610C/611C	153	129	118	58	–	–
SL612C	171	158	165	129	149	69

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NEW PRODUCT DATA

SL613C LIMITING AMPLIFIER/DETECTOR

The SL613C is a low noise limiting amplifier intended for use as an RF clipper, a limiting stage in IF amplifiers, or an RF Compressor in SSB transmitters. It contains a detector which may be used to detect AM but is particularly intended for use as an AGC detector. The amplifier, which has a gain of 12 dB when not limiting, has upper and lower 3 dB points of 150 MHz and 5 MHz respectively. It limits when its input exceeds 120 mV r.m.s. The detected output during limiting is 1 mA.

FEATURES

- Wide Bandwidth
- Low Noise
- Highly Symmetrical Limiting
- Large Signal Handling Capability

APPLICATIONS

- RF Clippers
- AGC Systems
- AM Detectors
- RF Compression in SSB Transmitters

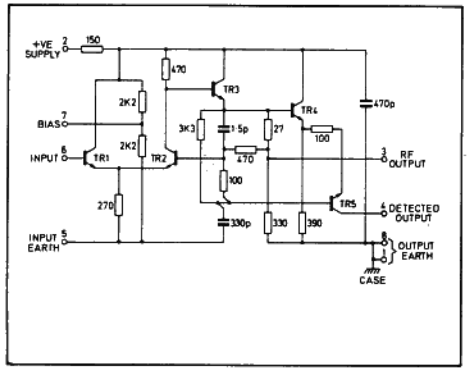


Fig. 1 Circuit diagram

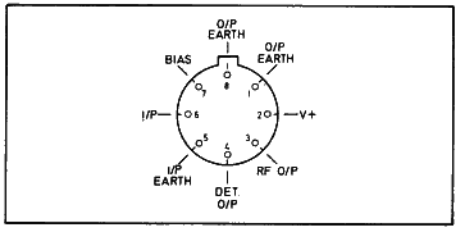


Fig. 2 Pin connections

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply +6V
Temperature +25°C
Pins 6 & 7 strapped together

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	3.3	4	4.6	–	30 MHz
Upper 3 dB frequency	120	150		MHz	
Lower 3 dB frequency		5	8	MHz	
Noise figure		4.5	5.5	dB	60 MHz 500Ω source
Supply current	11	15	20	mA	No signal
Limited RF o/p		1.25		V p-p	0.5 V input, 30 MHz
Detector current	0.85	1	1.25	mA	0.5 V input, 30 MHz
Maximum input before overload	1.5	1.75		V r.m.s.	30 MHz
Input impedance		5kΩ + 6pF			60 MHz. Open circuit o/p

OPERATING NOTES

The SL613C, like the SL610/11/12, is normally used with the input and bias pins connected directly together and the input applied through a capacitor. However, and again like the SL610/11/12, the bias may be decoupled and connected to the 'cold' end of a coil or tuned circuit, the input pin being connected to its 'hot' end or to a tap.

The supply rail is decoupled internally at RF but as the gain is dependent on supply voltage there should no appreciable LF ripple on the supply. Two separate earth connections are made in order to minimise the effects of common earth-lead inductance – such common earth-lead inductance can cause instability and care should be taken not to introduce it externally.

The RF output is capable of driving a load of 1kΩ in parallel with 10pF. If a capacitive load of more than 10pF is envisaged a resistor should be connected between the output pin and the load. Normally 50Ω is sufficient. The output should be isolated at DC by a capacitor.

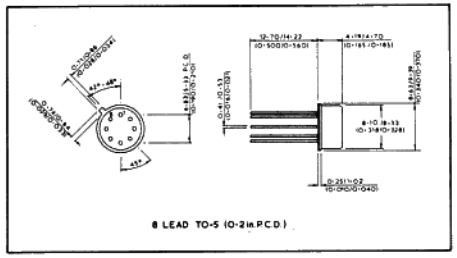
The detected output consists of a current out of pin 4, which is an NPN transistor collector. This pin must always be more than 3 volts more positive than earth, even if the detected output is not required (in which case it is best to strap pins 2 and 4).

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +175°C
Operating temperature	–55°C to +125°C
Supply voltage (pins 2 or 4)	+9V

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



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SL620C & SL621C

AGC GENERATORS

The SL621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL610C, SL611C and SL612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL610C and one SL612C amplifier and a suitable detector, the SL621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

The SL620C VOGAD (Voice Operated Gain Adjusting Device) is an AGC generator designed to work in conjunction with the SL630C audio amplifier (particularly when the latter is used as a microphone amplifier) to maintain the amplifier output between 70mV and 87mV rms for a 35 dB range of input. A one second 'hold' period is provided which prevents any increase of background noise during pauses in speech.

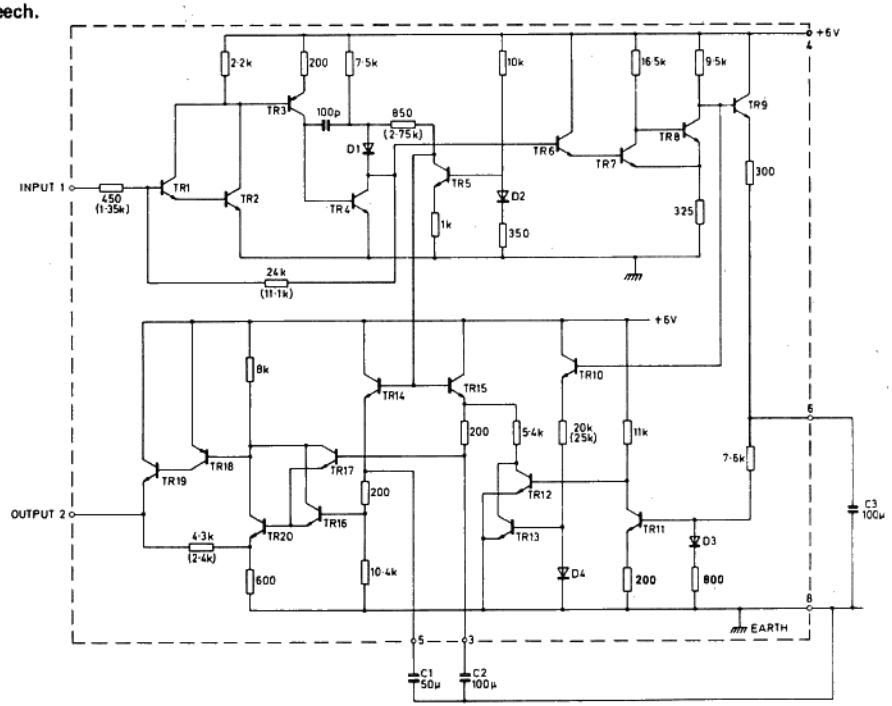


Fig. 1 Circuit diagram of SL620C and SL621C (Component values in brackets refer to SL620C)

DESCRIPTION

The operation of the SL621C is described with reference to the circuit diagram, Fig. 1, and Fig. 2 which illustrates the dynamic response of a receiver controlled by the SL621C.

The SL621C consists of an input AF amplifier TR1 – TR4 (3 dB point: 10KHz) coupled to a DC output amplifier, TR16 – TR19, by means of a voltage back-off circuit, TR5 and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

The detected audio signal at the input will rapidly establish an AGC level, via TR14, in time t_1 (see Fig. 2). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is the more sensitive.

If signals exist at the SL621C input which are greater than approximately 4mV rms they will actuate the trigger circuit TR6 – TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20 dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, so holding off TR12 via TR11. When the trigger pulses cease, C3 discharges and after t_5 turns on TR12. Capacitor C2 is discharged rapidly (in time t_4) via TR12 and so full receiver gain is restored. The hold time, t_5 is approximately one second with C3 = 100μF. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 2 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

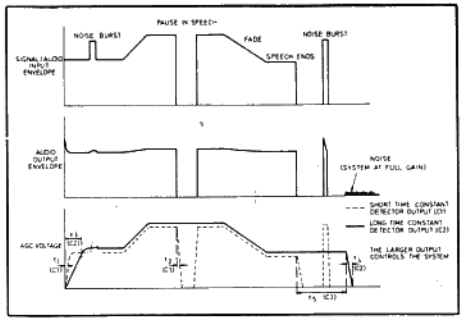


Fig. 2 Dynamic response of a system controlled by SL620C or SL621C AGC generator

OPERATING NOTES

The various time constants quoted are for C1 = 50μF and C2 = C3 = 100μF. These time constants may be altered by varying the appropriate capacitors.

An input coupling capacitor is required. This should normally be 0.33μF for an SL621C and about 1μF for an SL620C.

Fig. 3 shows how the SL621C may be connected into a typical SSB receiver.

Fig. 4 shows how the SL620C is used to control the gain of the SL630C audio amplifier. The operation of the SL620C is exactly the same as that of the SL621C and the diagram showing the dynamic response of the closed loop system, Fig. 2, is equally applicable to the SL630C/SL620C combination. Again, the time constants may be altered by varying the capacitor values.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least 500μF so that it is not affected by the current surge resulting from a sudden input on pin 1. The devices may be used with a supply of up to +9V.

In a receiver for both AM and SSB using an SL623C detector/Carrier AGC generator, the AGC outputs of the SL621C and SL623C may be connected together provided that no audio reaches the SL621C input while the SL623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output of an SL620 or SL621 should not exceed 15000pF or the impulse suppression will suffer.

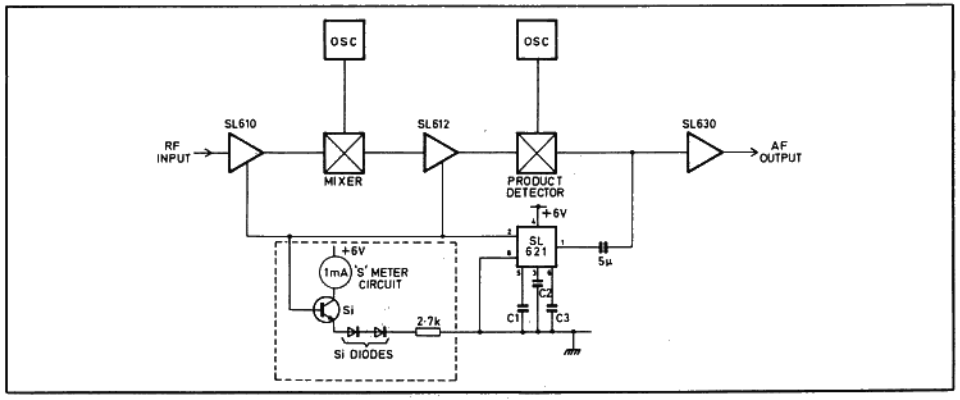


Fig. 3 SL621C used to control SSB receiver

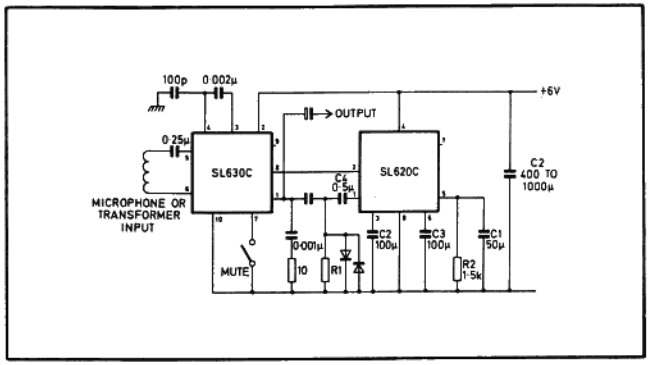


Fig. 4 SL620C used to control SL630C audio amplifier

ELECTRICAL CHARACTERISTICS SL 620C & SL 621C

Test conditions: Supply voltage = 6V
Temperature = +25°C
Input signal frequency = 1kHz

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
Input for 0.65V dc output	SL620C	55	70	85	mVrms	See Fig.5
Input for 1.5V dc output	SL620C	70	87	105	mVrms	See Fig.5
Input for 2.2V dc output	SL621C	6.0	7.0	10.0	mVrms	See Fig.6
Input for 4.6V dc output	SL621C	9.0	11.0	16.0	mVrms	See Fig.6
						Measurement accuracy 1 dB
*Fast rise time, t_1	Both		20	30	ms	0–50% full output
*Fast decay time, t_2	Both	150	200	250	ms	100%–36% voltage on C_1
						C_1 = 50μF
*Slow rise time, t_3	Both	150	200	300	msec	Time to output transition point
Input 3 dB point	Both		10		kHz	
Maximum fade rate	SL620C		0.22		V/s	
	SL621C		0.45		V/s	
						C_2 = 100μF
*Hold collapse time, t_4	Both	150	200	250	ms	Full-zero output
*Hold time, t_5	Both	0.75	1.0	1.25	s	C_3 = 100μF
A.C. ripple on output	Both		12	20	mVp-p	1kHz. Output open circuit
Maximum output voltage	SL620C	2.0			V	
	SL621C	5.1			V	
Quiescent current consumption	Both	2.5	3.1	4.1	mA	
Surge current	Both		30		mA	
Input resistance	SL620C	1	1.4	2	kΩ	
	SL621C	350	500	700	Ω	
Output resistance	SL620C	12	40	130	Ω	
	SL621C	20	70	230	Ω	

See Figure 2

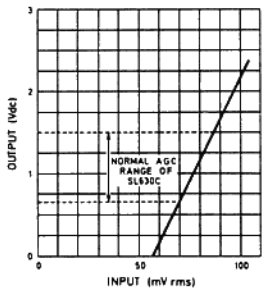


Fig. 5 Transfer characteristic of SL620C

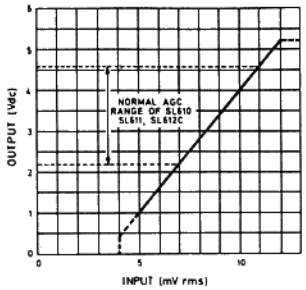


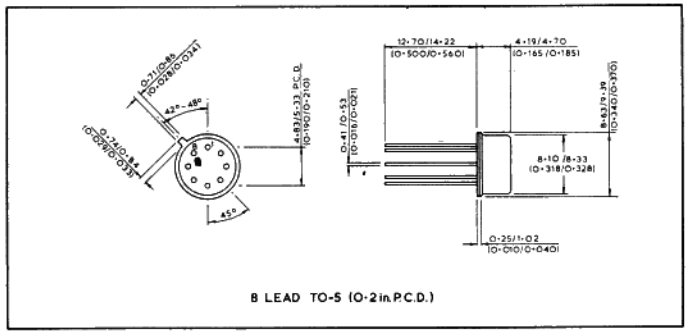
Fig. 6 Transfer characteristic of SL621C

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Free air operating temperature	−65°C to +165°C
Chip operating temperature	175°C
Chip-to-ambient thermal resistance	220°C/W
Chip-to-case thermal resistance	60°C/W
Supply voltage	12V

PACKAGE DETAILS

Dimensions are shown thus: mm(in)



8 LEAD TO-5 (0·2 in. P.C.D.)

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SL622C AF AMPLIFIER, VOGAD & SIDETONE AMPLIFIER

The SL622C is a silicon integrated circuit combining the functions of audio amplifier with voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low-sensitivity microphone and to provide an essentially constant output signal for a 60 dB range of input.

Additionally, a constant gain amplifier is incorporated which provides an amplitude-limited output for sidetone in mobile transmitter/receiver applications.

The encapsulation is a 10 lead TO-5 package and the device is designed to operate from a 6 to 12 volt supply, over a temperature range of −55°C to +125°C.

A voltage regulator produces an independent supply line at 4.7 Volts stabilised

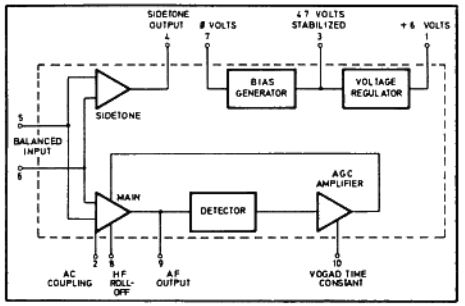


Fig. 1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test Conditions: Input frequency 1KHz; Supply voltage +6V; Temperature +25°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
VOGAD output level	55	90	110	mV rms	Balanced signal input 18mV rms
Sidetone output level	600	800	900	mV p-p	Balanced signal input 18mV rms
AF amplifier voltage gain	49	52	55	dB	Balanced signal input 72μV rms
Sidetone voltage gain	24.5	29	30.5	dB	Balanced signal input 72μV rms
Current consumption		14	16	mA	6V supply, input 1mV rms
consumption		24		mA	12V supply, input 1mV rms
Decay time — time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched down 20dB.		1.0		s	Original balanced signal input 18mV rms; R1 = 1 MΩ, C3 = 47μF, Test cct. as Fig.2
Attack time — time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched up 20dB.		20		ms	Original balanced signal input 1.8mV rms; R1 = 1 MΩ, C3 = 47μF, Test cct. as Fig.2
Total harmonic distortion at VOGAD output.		2		%	Balanced signal input 90mV rms
Differential input impedance.		300		Ω	
Single-ended input impedance.		180		Ω	
Sidetone output impedance		200		Ω	
AF amplifier output resistance		50		Ω	
VOGAD operating threshold (Whisper threshold)		100		μV rms @ I/P	

OPERATING NOTES

The SL622C incorporates a series regulator which will accept supply voltages between 6V and 12V and provides a supply line rejection of approximately 26 dB when operated from a 6V supply The supply line immunity increases with supply voltage.

The input stage is a differential class A-B stage with an AGC terminal. The accurate balance of the input stage give an overall common-mode rejection ratio of greater than 30 dB.

Typically the amplifier will handle differential input signals of up to 375mV p-p and unbalanced signals of up to 50mV p-p. When used in the unbalanced mode either pin 5 or pin 6 may be used as the input, the other being decoupled to earth.

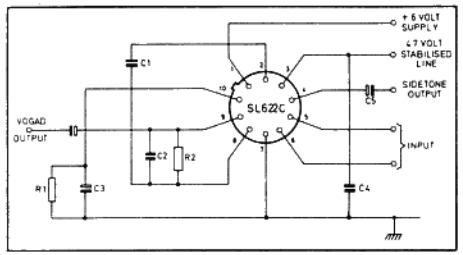


Fig. 2 Connection diagram for SL622C used as a microphone amplifier.

Fig. 2 shows the SL622C when used as a balanced microphone amplifier. The LF cut-off of the amplifier is set by C1 – and also by the values of coupling capacitors to the input pins (pin 5 and pin 6); coupling capacitors should be used if the d.c. potential of the input is not floating with respect to earth.

The HF cut-off is set by C2. The VOGAD threshold may be increased by connecting an external conductance between pins 8 and 9. The threshold is increased by approximately 20 dB for 1 millimho of conductance, the value of C2 should be adjusted in conjunction with any threshold alteration in order to obtain the desired bandwidth.

C3 and R1 set the attack and decay rates of the VOGAD. C3 = 47μF and R1 = 1Mohm gives an attack time constant (gain increasing) of 20 millisecs and a decay rate of 20 dB/sec. C1 = 2.2μF and C2 = 4.7nF give a 3 dB bandwidth of approximately 300Hz to 3kHz.

The amplifier can be muted by applying +4V to pin 10, but when the voltage is removed either C3 must be discharged or there will be an appreciable delay before the circuit functions normally again.

C4 is used for RF decoupling of the stabilised line. AF decoupling may be applied to improve supply line rejection and sidetone linearity.

The VOGAD and sidetone steady-state transfer characteristics are shown in Figs. 3 and 4.

ABSOLUTE MAXIMUM RATINGS

Continuous supply voltage (positive)	12V ± 0.5V
Storage temperature	−55°C to + 175°C
Ambient temperature (6V operating)	−55°C to + 125°C
(12V operating)	−55°C to + 100°C

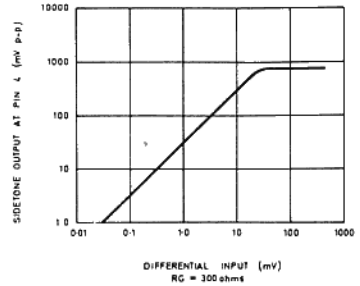


Fig. 3 Sidetone output characteristics.

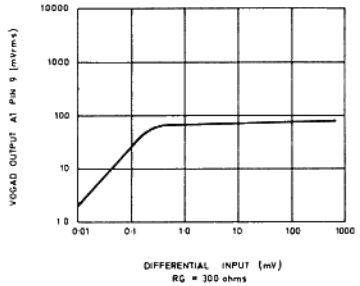
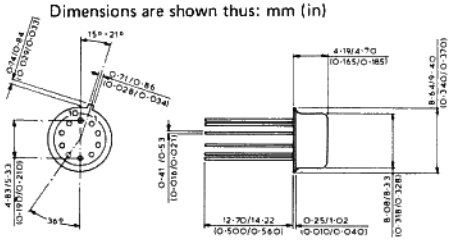


Fig. 4 VOGAD – output characteristics (1kHz sinewave input).

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



10 LEAD TO-5

Pin	Function
1	+6 volts supply
2	A.C. coupling
3	+4.7V decoupling
4	Sidetone o/p
5, 6	Balanced signal input
7	OV
8	HF Roll off
9	AF o/p
10	VOGAD time constant.

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SL600 SERIES
COMMUNICATIONS CIRCUITS

SL623C
AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL610C, SL611C and SL612C RF and IF amplifiers. It is complementary to the SL621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL610C and one SL612C amplifier, the SL623C will maintain the output within a 5 dB range for a 90 dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100 mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies. The encapsulation is a 10 lead TO-5 package and the device is designed to operate from a 6 volt supply, over a temperature range of −55°C to +125°C.

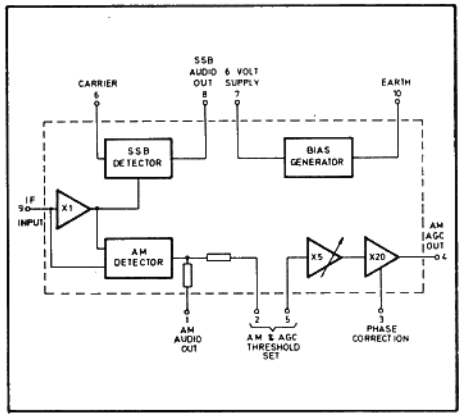


Fig. 1 Block Diagram

ELECTRICAL CHARACTERISTICS @ SUPPLY = +6V, T_{amb} = + 25°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
SSB Audio Output	25	30	42	mV rms	Signal Input 20mV rms @ 1.748 MHz. Ref. Signal Input 100mV rms @ 1.750 MHz
AM Audio Output	45	55	64	mV rms	Signal Input 125mV rms @ 1.75 MHz. Modulated to 80% @ 1 kHz.
AGC Range (change in input level to increase AGC output voltage from 2.0V to 4.6V)			5	dB	Initial signal input 125mV rms at 1.75 MHz. Mod. to 80% at 1 kHz Output Set with 10kΩ pot between pins 2 & 5 to 2.0V.
Quiescent Current Consumption		9	11	mA	Output open circuit
Max. operating frequency		30		MHz	
Change of SSB audio output with temperature +85°C		−0.5		dB	Signal Input 20mV rms @ 1.784 MHz. Ref. signal input 100mV rms @ 1.75 MHz.
−40°C		+0.5		dB	
Change of AM audio output with temperature +85°C		−0.25		dB	Signal Input 125mV rms @ 1.75 MHz Modulated to 80% @ 1 kHz.
−40°C		−0.25		dB	

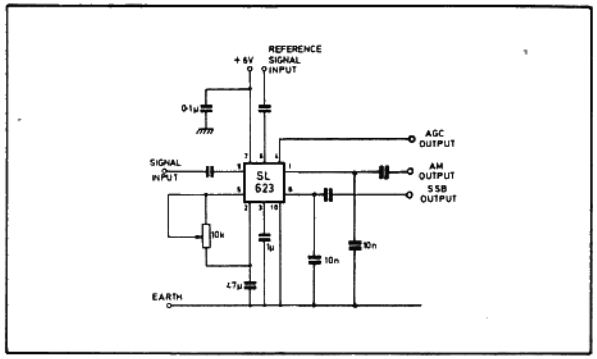


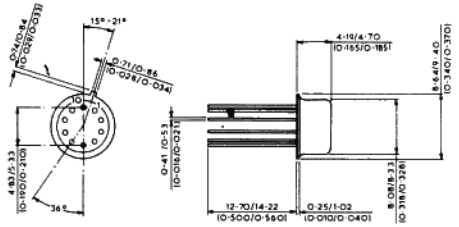
Fig. 2 Typical circuit using the SL623C as signal detector and AGC generator.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Ambient operating temperature	−55°C to +125°C
Supply voltage	−0.5V to +12V

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



10 LEAD TO-5

Pin	Function
1	AM Audio Output.
2	AM AGC Threshold Set.
3	Phase Correction.
4	AGC Output.
5	AM AGC Threshold Set.
6	Reference Signal Input.
7	+6V Supply.
8	SSB Audio Output.
9	Signal Input.
10	O V

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NEW PRODUCT DATA

SL624C MULTIMODE DETECTOR

The SL624C is a complex integrated circuit designed for use as a detector of AM, FM, SSB or CW, acting respectively as a synchronous detector, a quadrature detector and a product detector with built-in oscillator. It also contains a voltage-controlled gain system and a separate audio amplifier capable of driving a single transistor output stage.

A major advantage of the SL624C as an AM detector is that unlike an envelope-detector, it does not give an output on broad band IF noise when used in a typical receiver following a block filter and a broadband IF amplifier.

FEATURES

- Demodulates FM, AM, SSB and CW
- Operates up to 30 MHz (Typ)
- Voltage-Controlled Audio Gain
- Separate Audio Driver

APPLICATIONS

- Mobile Transceivers
- HF Transceivers
- VHF Transceivers

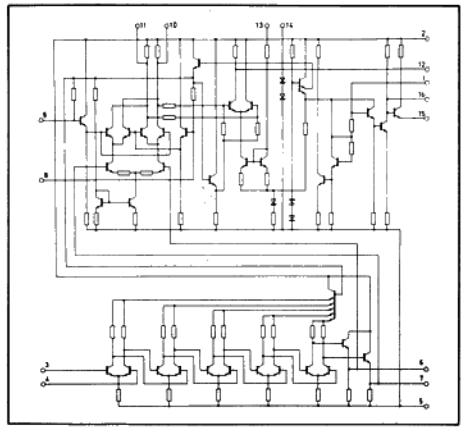


Fig. 1 Circuit diagram

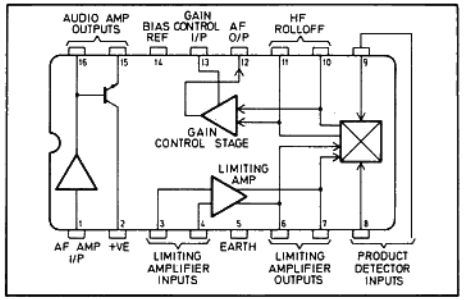


Fig. 2 Block diagram and pin connections (top)

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply +12V
Temperature +25°C (unless otherwise stated)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	9	12	15	V	
Current drain		23		mA	
Minimum input for synchronous AM detector					
+25°C		1		mV r.m.s.	9 MHz input
−55°C to +125°C		5			
Minimum input for limiting					
+25°C		100		μV r.m.s.	9 MHz input
−55°C to +125°C		300			
Detector audio gain range		80		dB	
Audio amplifier input R	20	50		kΩ	
Audio amplifier voltage gain		4		—	
Maximum operating frequency (limiting amplifier)		30		MHz	

OPERATING NOTES

Figs. 3, 4 and 5 show the SL624C used, respectively, as a synchronous AM detector, a quadrature FM detector and a self-oscillating product detector. It is evident that a multimode receiver may be made either by switching the components around one SL624C with relays or diodes, or by using three SL624Cs, one per mode.

The supply to the SL624C should be decoupled at HF by a 0.1 μF capacitor sited as near as possible to pins 2 and 5.

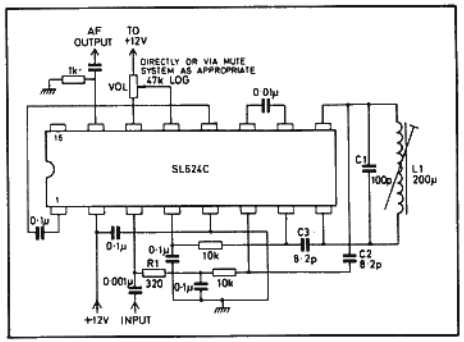


Fig. 4 FM quadrature detector

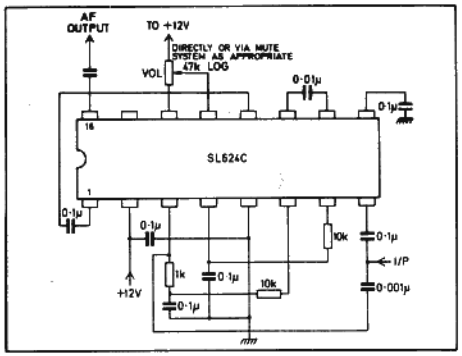


Fig. 3 Synchronous AM detector

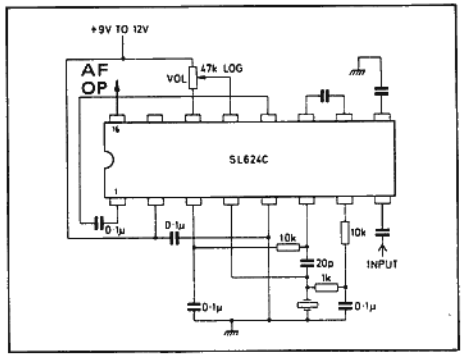


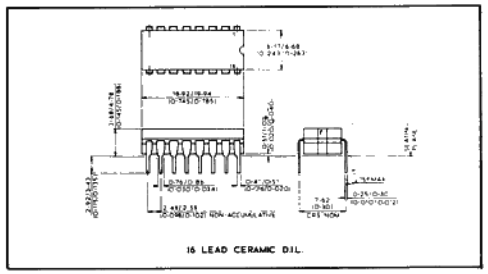
Fig. 5 Self-oscillating product detector

ABSOLUTE MAXIMUM RATINGS

Storage temperature:	–55°C to +175°C.
Operating temperature:	–55°C to +125°C.
Supply voltage (pin 2):	+18V.

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



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SL630C

MICROPHONE/HEADPHONE AMPLIFIER

The SL630C is designed specifically for use as a microphone or headphone amplifier. It has a voltage gain of 100, will accept balanced or unbalanced inputs, and can deliver up to 250mW output from a class AB push-pull output stage.

A gain control facility with a logarithmic law allows a.g.c. to be applied when the device is used as a microphone amplifier, and also allows remote volume control with a linear potentiometer. Gain reduction of 100 dB may be obtained

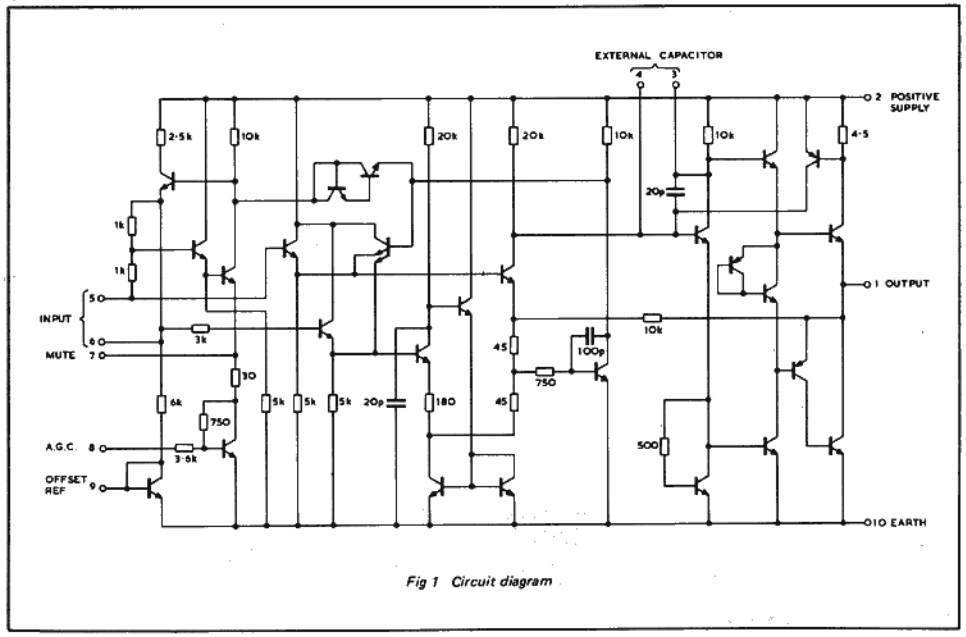


Fig 1 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions: Temperature = +25°C
Signal Frequency = 1kHz
Supply = 12V (unless otherwise stated)

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
Differential input voltage gain	38	40	42	dB	Input 1mVrms
Single ended input voltage gain	43	46	49	dB	Input 1mVrms
Maximum output voltage		1.2		Vrms	6V supply
	2.5	2.8		Vrms	12V supply
Maximum output power		See Fig. 6			0.5% distortion
Quiescent current (See also Fig. 6)			5	mA	6V supply
			13	mA	12V supply
Differential input impedance	1.0	2.0	3.6	kΩ	
Single ended input impedance		1.0	1.8	kΩ	
Output impedance		1.5	3.0	Ω	
Gain control range (See Fig. 5)	60	100		dB	
Maximum input (with gain reduced)		50		mVrms	10% distortion
Short circuit output current		110	200	mA	Irrespective of supply

OPERATING NOTES

Frequency Response

As with most small-signal integrated circuits, the inherent bandwidth of the SL630C is quite large. It extends from low audio frequencies up to approximately 0.5 MHz, unless restricted by a roll-off capacitor (C1) connected between pins 3 and 4. The approximate upper cut-off frequency is then given by

$$\omega_c \simeq \frac{10^8}{C1}$$

where C1 is in picofarads

Muting

This can be achieved, in any application, by switching pin 7 directly to the negative rail

Microphone Amplifier

Fig. 2 shows the SL630C used with a balanced input on pins 5 and 6. If the load resistance increases with frequency it is necessary to stabilize the output circuitry. This is accomplished with 10Ω in series with 1nF connected between pin 1 and earth. The earth return to pin 10 must not share any common leads, particularly with the input. Decoupling pins 2 and 6 should follow normal engineering practice.

Headphone Amplifier

Fig. 3 shows the SL630C in a circuit suitable for powering a headset. The input is an unbalanced source connected to pin 5 and the device is decoupled at pins 1, 2 and 6 in the same manner as the microphone amplifier.

Manual gain adjustment using the remote gain control facility is also shown. It should be noted that the connection to pin 9 eliminates the 'dead' portion of the volume control range caused by the delayed attenuation characteristic shown in Fig. 5. R1 and R2 are chosen with regard to Fig. 5 to give the desired control range.

The input impedance at pin 8 is 3.6 kΩ.

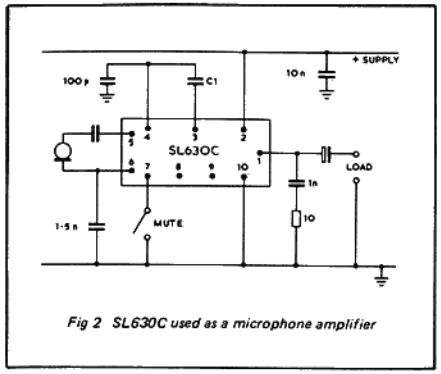


Fig 2 SL630C used as a microphone amplifier

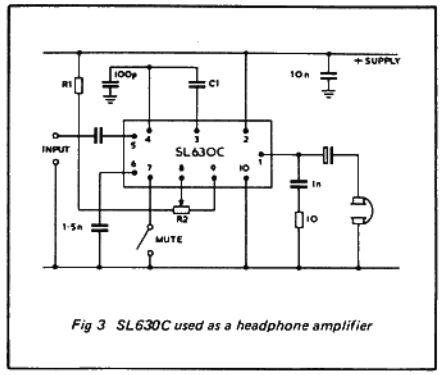


Fig 3 SL630C used as a headphone amplifier

Automatic Gain Control

To apply a.g.c., an SL620C should be used as shown in the circuit of Fig. 4. This will give effective gain control with a low audio-frequency cut-off of 200 Hz and a control response time of approximately 20 ms.

To preserve low-frequency stability and prevent motor-boating, C4 should not exceed the value given and, whilst R1 should not exceed 300Ω, the time constant C3R1 must not be greater than 800 μs.

R2 is non-essential, but is useful if the input is likely to contain a large component below 300 Hz

C2 should be used if the power supply has a source impedance of more than a few ohms or is connected by long wires.

The system should not be tested with sinewave inputs below 300Hz as such signals can give rise to delay effects not produced by speech waveforms.

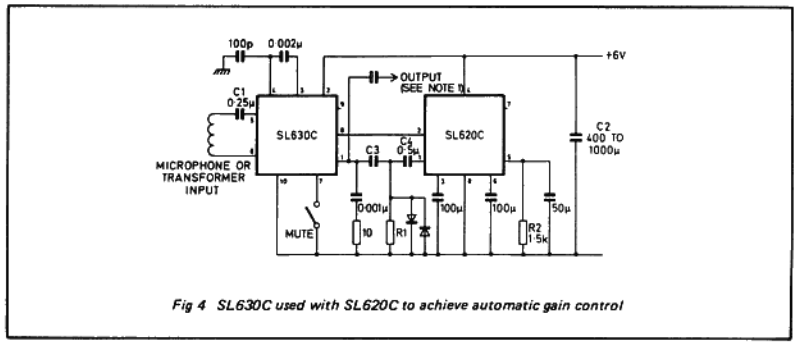


Fig 4 SL630C used with SL620C to achieve automatic gain control

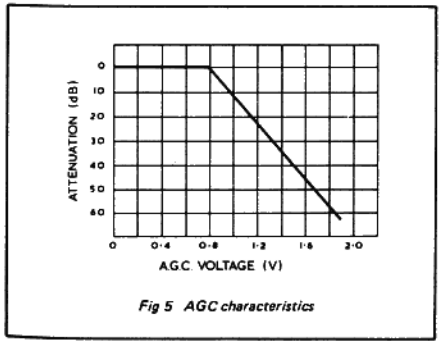


Fig 5 AGC characteristics

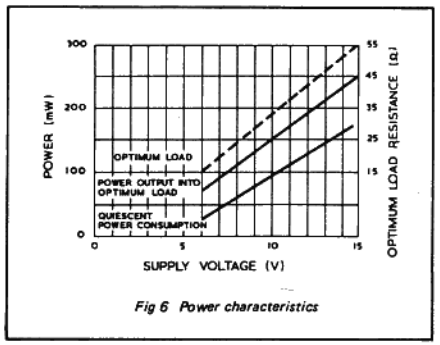


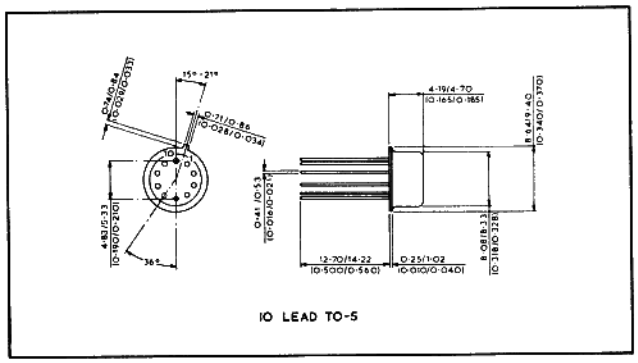
Fig 6 Power characteristics

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Free air operating temperature range	
6V supply	−55°C to +125°C
12V supply	−55°C to +100°C
Supply voltage	+18V

PACKAGE DETAILS

Dimensions are shown thus : mm (in)



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SL640C & SL641C

DOUBLE BALANCED MODULATORS

The SL640C is designed to replace the conventional diode ring modulator, in RF and other communications systems, at frequencies of up to 75MHz. It offers a performance competitive with that of the diode ring while eliminating the associated transformers and heavy carrier drive power requirements.

At 30 MHz, carrier and signal leaks are typically −40dB referred to the desired output product frequency. Intermodulation products are −45dB with a 60 mV rms input signal

The SL641C is a version of the SL640C intended primarily for use in receiver mixer applications for which it offers a lower noise figure and lower power consumption. No output load resistor is included and signal leakage is higher, but otherwise the performance is identical to that of the SL640C

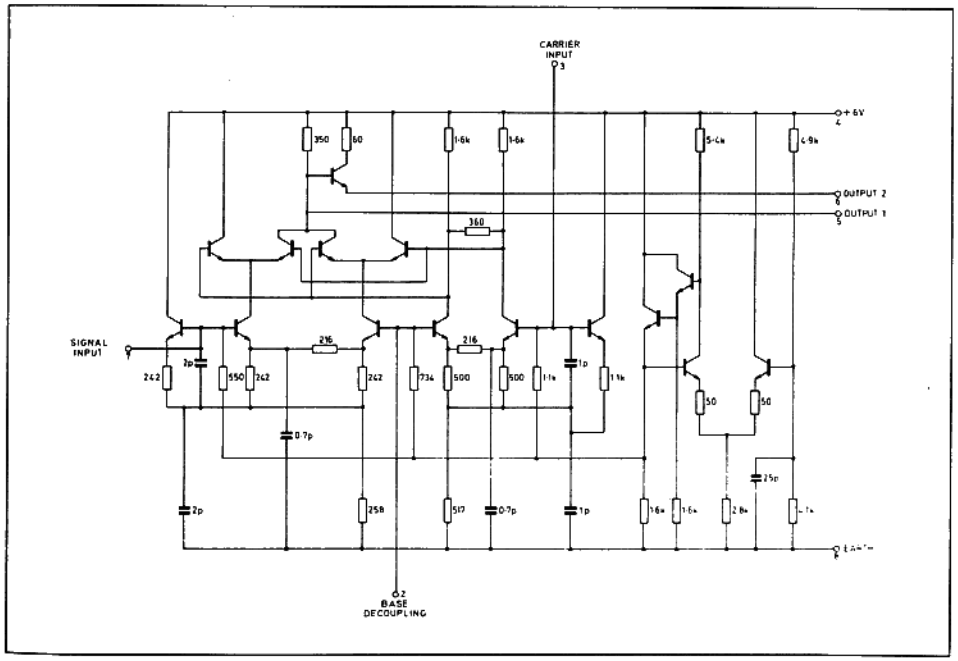


Fig. 1 Circuit diagram of SL640C

ELECTRICAL CHARACTERISTICS SL640C & SL641C

Test conditions: Supply voltage = +6V
Temperature = +25°C unless otherwise stated

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
Conversion gain	SL640C	−2	0	+2	dB	
Signal leak	SL640C		−40	−20	dB	Signal: 70mVrms, 1.75MHz Carrier: 100mVrms, 28.25MHz Output: 30MHz
= Signal output / Desired sideband output						
Carrier leak	SL640C		−40	−20	dB	
= Carrier output / Desired sideband output						
Intermodulation products	SL640C		−45	−35	dB	Signal 1: 42.5mVrms, 1.75MHz Signal 2: 42.5mVrms, 2MHz Carrier: 100mVrms, 28.25MHz Output: 29.75MHz
Conversion transconductance	SL641C	2.2	2.5	3.5	mmho	
Signal leak	SL641C		−18	−12	dB	Signal: 70mVrms, 30MHz Carrier: 100mVrms, 28.25MHz Output: 1.75MHz
Carrier leak	SL641C		−25	−12	dB	
Intermodulation products	SL641C		−45	−30	dB	Signal 1: 42.5mVrms, 30MHz Signal 2: 42.5mVrms, 31MHz Carrier: 100mVrms, 28.25MHz Output: 3.75MHz
Carrier input impedance	Both		1kΩ & 4pF			
Signal input impedance	SL640C		500Ω & 5pF			
	SL641C		1kΩ & 4pF			
Output impedance (see Operating Notes)	SL640C		350Ω & 8pF			Output 1
	SL641C		8		pF	
Max. input before limiting	SL640C		210		mVrms	
	SL641C		250		mVrms	
Quiescent current consumption	SL640C		12	16	mA	
	SL641C		10	13	mA	
Noise figure	SL640C		15		dB	
	SL641C		12		dB	
Signal leak variation	Both		±2		dB	
Carrier leak variation	Both		±2		dB	−55°C to +125°C
Conversion gain variation	Both		±1		dB	

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Supply voltage	+9V
Free air operating temperature range	−55°C to +125°C

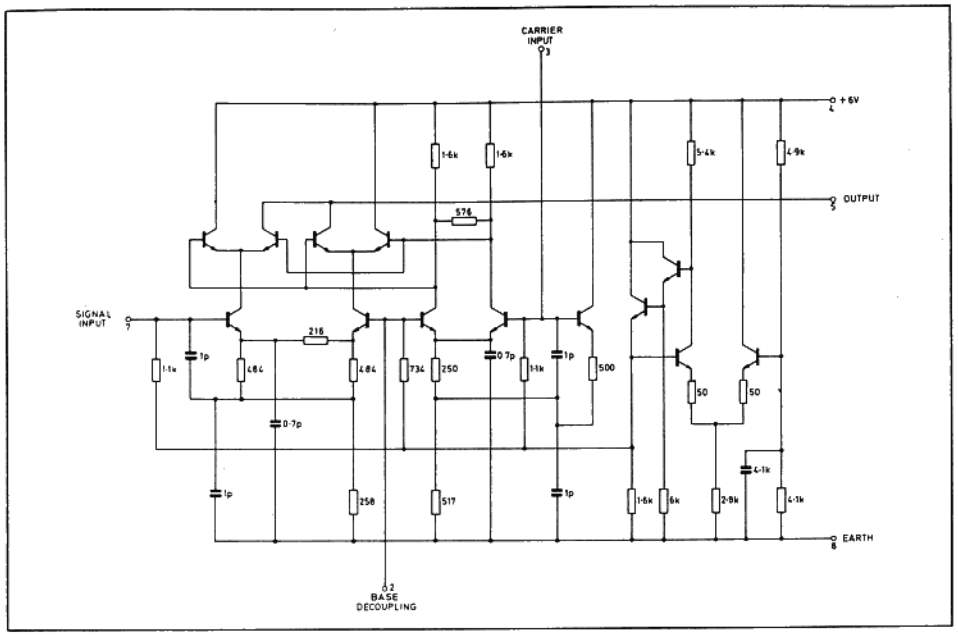


Fig. 2 Circuit diagram of SL641C

OPERATING NOTES

The SL640C circuit requires input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see electrical characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance.

Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at pin 2 would give rise to poor rejection figures and to distortion.

If the emitter follower is used, an external load resistor must be provided to supply emitter current. The quiescent output voltage from the emitter follower (pin 6) is +4.6V. To achieve maximum rejection figures at high frequencies, pin 1 (which is connected to the header) should be connected to earth and effective HT decoupling should be employed. The DC impedance should not exceed 800 ohms.

The SL641C is very similar to the SL640C but has, instead of a voltage output, a current output to enable a tuned circuit to be directly connected.

If both output sidebands are developed across the load (i.e. wideband operation), the AC impedance of the load must be less than 800Ω. If the output at one sideband frequency is negligible, the AC impedance may be raised to 1.6kΩ. It may be further raised if it is not desired to use the maximum input swing of 210mV rms.

The SL640C/641C may be used with supply voltages of up to +9 volts with increased dissipation.

Signal and carrier leaks may be minimised with 10kΩ potentiometers and 330kΩ resistors connected as shown in fig.3. R1 is adjusted to minimise signal leak; R2 to minimise carrier leak.

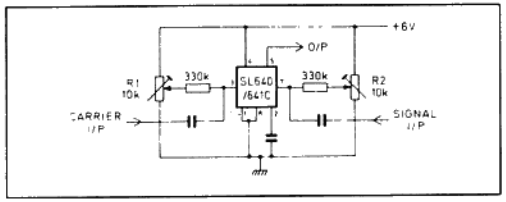
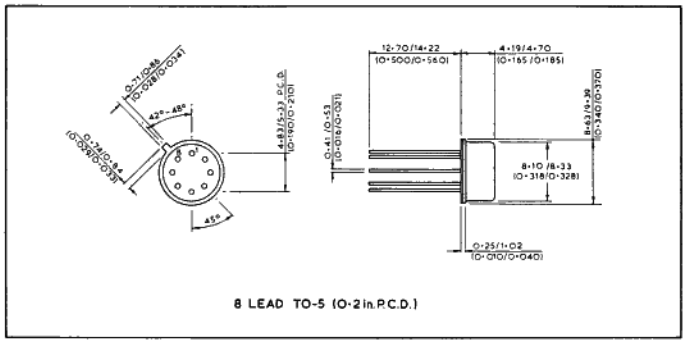


Fig. 3 Signal and carrier leak adjustments

PACKAGE DETAILS

Dimensions are shown thus: mm(in)



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SL645C SQUARE LAW DEVICE

The SL645C is a monolithic bipolar integrated circuit which functions as a two-quadrant square law element. When used as a frequency doubler, it will operate satisfactorily up to input frequencies in excess of 200 MHz. In addition, a mean square detector is provided which may be used as part of an AGC loop to control the magnitude of the input signal to the integrated circuit.

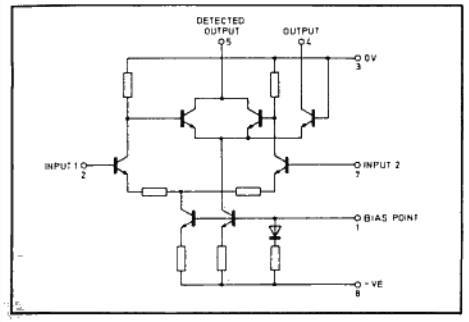


Fig.1 Circuit Diagram

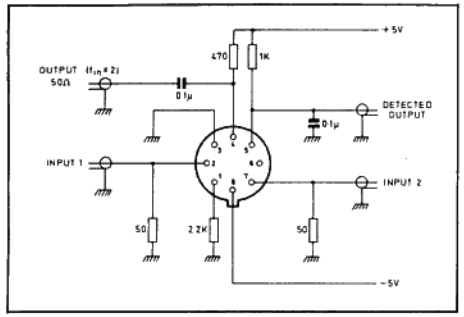


Fig.2 Test Circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (See Fig.3)

Supplies	± 5V
V_{in}	600 mV p-p
T_{amb}	+25°C ± 5°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions	
Mean output current			150	μA	V_{in} = 0	Pin 5
Mean output current	250			μA	f_{in} = 40MHz	Pin 5
Output current p-p	200			μA	f_{in} = 80MHz	Pin 4
		200		μA	f_{in} = 200MHz	Pin 4
Input signal suppression	10			dB	f_{in} = 80MHz	Pin 4
		8		dB	f_{in} = 200MHz	Pin 4
Supply current			5	mA		
Input resistance		10		kΩ	$f_{in} < 5$MHz	
Output capacitance		0.5		pF		Pin 4

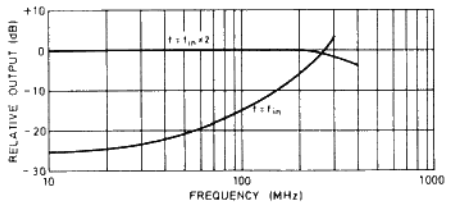


Fig.3 Output Level v. Frequency

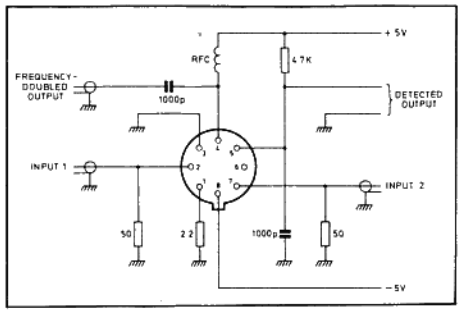


Fig.4 Typical Application Circuit

OPERATING NOTES

Inputs

Differential inputs are provided but the circuit may be single input driven with no degradation of performance. The unused input should be connected via a low resistance (50Ω) to earth.

Outputs

Either pin 4 or pin 5 can be used as output. Pin 4 has the lowest capacitance and should be used as the output if high frequency operation is required. The quiescent current drawn by pin 5 is approximately one tenth of that drawn by pin 4 and this current increases with the input voltage, whereas that drawn by pin 4 decreases. Pin 5 would therefore normally be used for a detected output. Fig.4 shows a typical application. The smoothing capacitor between pin 5 and earth will vary depending on the operating frequency.

High Frequency Use

For high frequency operation (f_{in}> 100 MHz) careful layout and screening should be employed to avoid direct feedthrough of the input frequency. The shunting effect of the output capacitance must also be eliminated by the use of low impedance or tuned loads.

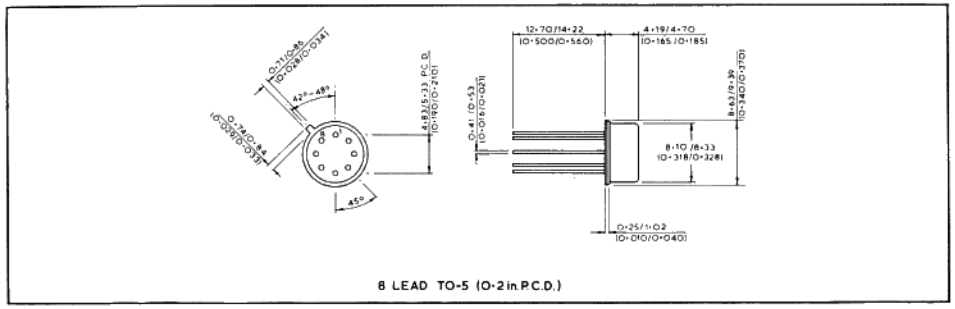
The output current may reduce by 50μA if the device is operated within the temperature range −10°C to +50°C.

ABSOLUTE MAXIMUM RATINGS

Voltage between any of pins 2, 4, 5, 7 & 8 to earth	10V
Voltage between pin 4 or pin 5 to −ve supply	20V
Storage temperature range	-55°C to +175°C
Free air operating temp.	−55°C to +125°C
Chip operating temp.	175°C
Chip-to-ambient thermal resistance	Chip-to-ambient 220° C/W
Chip-to-ambient thermal resistance	60° C/W

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



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Appendices

The following appendices contain information of value to users of SL600 devices in communications systems but which cannot logically be included in the body of the manual.

APPENDIX A Reference list of Plessey Semiconductors integrated circuits

APPENDIX B An SSB transceiver

APPENDIX C A high-performance morse keyer

APPENDIX D A multimode transceiver

Appendix A

This information consists of brief references to various Plessey Semiconductors integrated circuits which have either been mentioned in the manual or are otherwise relevant to communications engineering,

SL300 Series

NPN Transistor Arrays, in various configurations, intended for applications where close parameter matching and thermal tracking are of prime importance.

SL360C

Matched pair of NPN transistors with very high f_T (typically 2.5 GHz) and low capacitances.

SL362C

Matched pair of NPN transistors for low noise, high frequency, applications. Typical noise figure at 60 MHz is less than 1.6 dB, f_T is typically 1.5GHz.

SL3045

The SL3045 is a monolithic array of five general purpose high frequency transistors arranged as a differential pair and three isolated transistors. The transistors feature a V_{BE} matching of, typically, better than ± 5mV between any pair, an f_T of 600 MHz, and a low noise figure – all with the full military temperature specification. Input offset current for the differential pair is 2μA max. at a collector current of 1mA.

SL415A & SL414A

The SL415A and SL414A are robust high gain audio power amplifiers each with a separate pre-amplifier. The circuits, which have been optimized to give maximum reliability, have power outputs of 5W and 3W, respectively.

SL510C & SL511C

The SL510C is a bipolar integrated circuit combining the functions of RF detection and video amplification. The device is sectionalised to enable the RF detector to be used with or without the accompanying video amplifier.
The detector will accept carrier wave signals over a bandwidth from DC to 100 MHz. The incremental gain is typically 11 dB with a video bandwidth of DC to 24 MHz. The circuit will handle pulse widths down to 16ns and the dynamic range is 31 dB.
Although the primary area of application is in the radar field for RF pulse detection, the wide dynamic range of the SL510C also makes it suitable for detection of amplitude modulation.
The SL511C is of similar design, but has an incremental gain of typically 16 dB over a bandwidth of DC to 14 MHz. The dynamic range is maintained at 28 dB.

SL530C

The SL530C is a monolithic non-linear integrated circuit designed to realise a logarithmic transfer function in high-gain amplifier strips at frequencies between 4 and 80 MHz. The device is so designed that input signal phase information is retained. A typical dynamic range of 70 dB can be achieved over a bandwidth of 10 MHz.

SL650C

The SL650C is a versatile integrated circuit capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650C, with all parameters accurately controllable; the circuit can also be used to generate precise waveforms at frequencies up to 0.5 MHz.

SL1030C

The SL1030 is a silicon integrated circuit 200 MHz wideband amplifier. External components enable users to tailor the characteristics of the amplifier for particular applications. The gain can be selected between 20 and 60 dB; the input impedance can be 50Ω, 75Ω or 1kΩ, and the compromise between current consumption and output swing can be selected by the external components.

SP600 Series

The SP600 series is a family of high-speed divider integrated circuits for use in very high frequency measurement and communications equipment. Circuits are available with a variety of division ratios (from ÷2 to ÷32), operating frequencies from DC to 1 GHz and ECL/TTL compatible outputs – in both commercial and military temperature ranges.

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SL600 SERIES
COMMUNICATIONS CIRCUITS

Appendix B
AN SSB TRANSCEIVER USING SL600 SERIES INTEGRATED CIRCUITS

This note describes the heart of a single sideband transceiver for use in the range of 10 kHz to 500 MHz. The unit is constructed on a single printed circuit board and requires only a local oscillator, linear amplifier, pre-selector, microphone and loudspeaker to complete the transceiver.

RECEIVER

The receiver is a single conversion superheterodyne with a 9 MHz intermediate frequency. In order to improve the cross-modulation characteristics there is no RF amplification, high gain being provided by the IF stages.

The input mixer is an ANZAC MD108 diode ring, which is used in order to obtain good large signal performance. The mixer input (pins 3 and 7) is obtained from a pre-selector, which prevents the image frequency being received. The local oscillator signal is applied to pin 8 of the MD108 at a level of about +7 dBm (500 mV). A toroidal transformer is used to match the 50Ω output of the mixer to the crystal filter. IF amplification is provided by three cascaded SL612Cs, which are followed by an SL640C used as a product detector. The carrier insertion oscillator is an FET which delivers 100 mV r.m.s. into the product detector. The audio amplifier, an SL630C, provides 100 mW output into a 40Ω loudspeaker; audio gain control is by means of a DC potential applied to pin 8 of the SL630 by a 5kΩ potentiometer in series with a 5kΩ resistor, as shown in Fig.1.

Automatic gain control is provided by an SL621C a.g.c. generator, the transistor TR2 being used to buffer the output of the SL621C so that an 'S' meter may be driven from the emitter of TR2 if required. C16, C18 and C20 are kept low (4700pF) in order to retain the ignition suppression characteristics of the SL621C system.

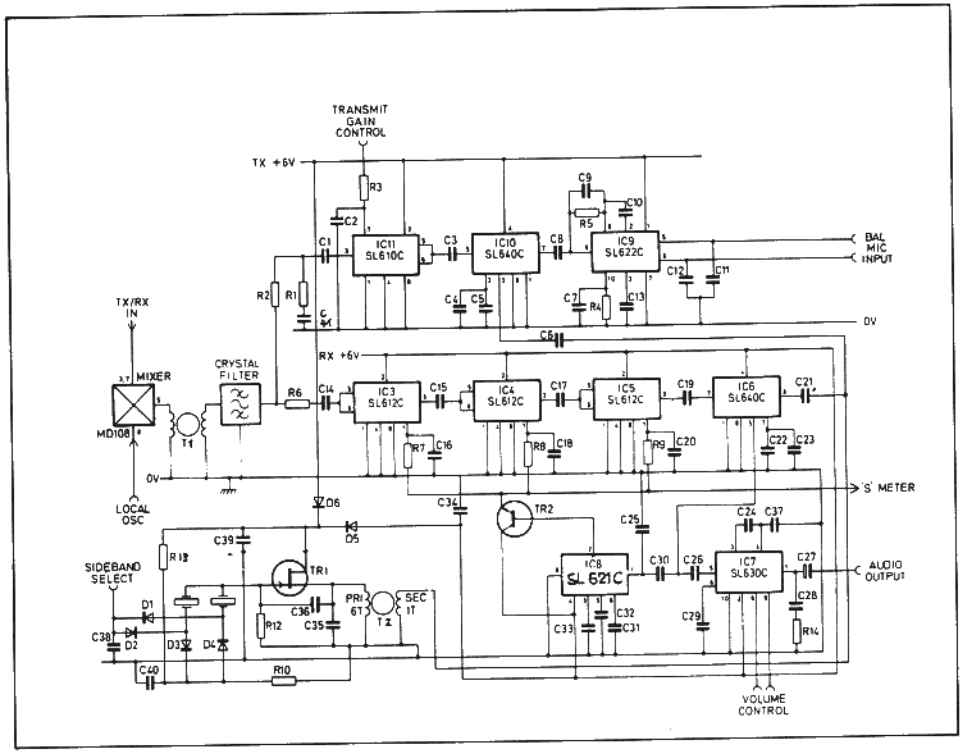

Fig.1 Circuit diagram of PCB

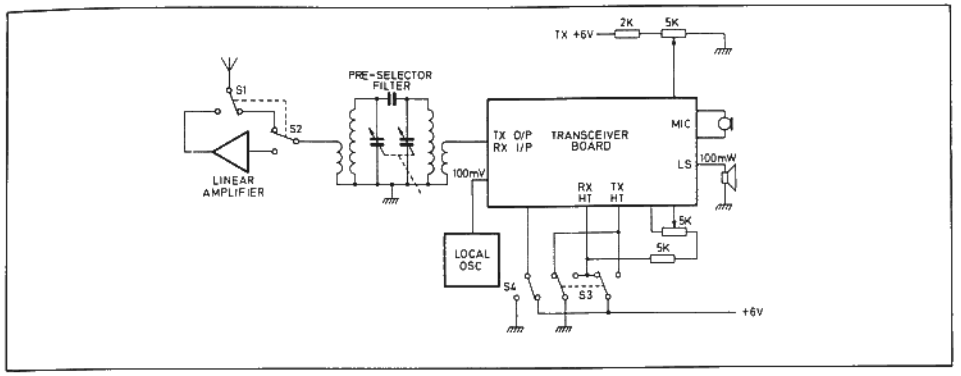

Fig.2 Block diagram of transceiver

TRANSMITTER

The transmitter is also single conversion. It generates SSB at 9 MHz by the filter method using the same crystal filter as the receiver. An SL622C is used as the microphone pre-amplifier; this device has its own a.g.c. which automatically adjusts the output to suit the SL640 balanced modulator.

The SL640C is followed by an SL610C amplifier which has ALC (derived from later stages of the transmitter) or a DC RF gain control applied to pin 7 of the SL610C. Resistors R1 and R2 (see Fig.1) provide the correct match to the filter.

The diode ring mixes the 9 MHz SSB with the local oscillator to produce the required output frequency (and of course the image frequency which afterwards must be removed).

The carrier injection is provided by an FET oscillator, with 2 diode-switched crystals for upper and lower sidebands.

CONSTRUCTION

The circuit board is single-sided, with two wire links on the top – one in the receive HT line the other the transmit HT line. The layout of this transceiver is critical; change of printed circuit design is not recommended as this could lead to instability

Transformer T1 is made from four 2-inch lengths of 26 SWG wire twisted together, the twisted wire is then used to wind two turns on a CR 071–8A core. The ends are then separated and three windings connected in series for form the secondary the primary being the remaining winding.

The board may be used as a receiver by omitting the following components: R1 to R5 inclusive, C1 to C13 inclusive and the three integrated circuits used in the transmitter. A 500Ω resistor should be connected between the crystal filter output and earth.

The 100 mw audio output has been found adequate for most purposes but if extra power is required it could be obtained from a Plessey SL414 audio amplifier external to the board. In practice the sensitivity of the receiver is satisfactory up to 30 MHz but above this frequency an RF amplifier is useful to take advantage of the lower atmospheric noise

PARTS LIST

Circuit Reference	Value	Rating	Type
R1, R3, R7-9, R11	100 Ω	1/8 W	Hi-stab carbon film
R2	430Ω	1/8 W	Hi-stab carbon film
R4	30kΩ	1/8 W	Hi-stab carbon film
R5	1kΩ	1/8 W	Hi-stab carbon film
R6	50Ω	1/8 W	Hi-stab carbon film
R10,R13	330Ω	1/8 W	Hi-stab carbon film
R12	100kΩ	1/8 W	Hi-stab carbon film
R14	10Ω	1/8 W	Hi-stab carbon film
C1,C2,C3,C4,C11, C12,C22,C29	1nF		Wee Con
C5,C8,C23,C26	10μF	6.3V	Plessey tantalum bead 402/1/54006/130
C6	100pF		Erie Hi-K submin. tubular
C7,C32	47μF	6.3V	Plessey tantalum bead 402/1/54009/100
C9	4,7nF		Wee Con
C10	2μF	16V	Plessey tantalum bead 402/1/54006/090
C13,C25,C39,C40	0.1μF		Wee Con
C14,C15,C17, C19,C21,C37	100pF		Ceramic
C16,C18,C20,C24	4.7nF		Wee Con
C27,C31,C33	100μF	6.3V	Plessey tantalum,bead 402/1/54017/040
C28,C38,C41	10nF		Wee Con
C30	1μF	35V	Plessey tantalum bead 402/1/54006/070
C34	400μF	16V	Miniature aluminium electrolytic
C35,C36	68pF		Ceramic
D1–D6	1N4148 –		Semitron
TR1	2N3819		
TR2	2N706		
T1+T2	CR071-8A		ITT-CORE

SCALE $\sqrt{2}:1$

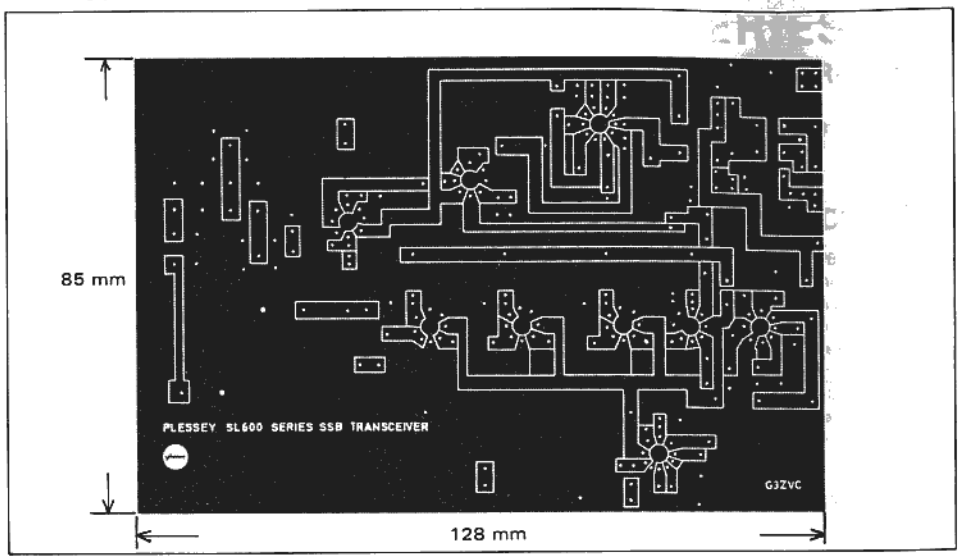

Fig.3 PCB layout

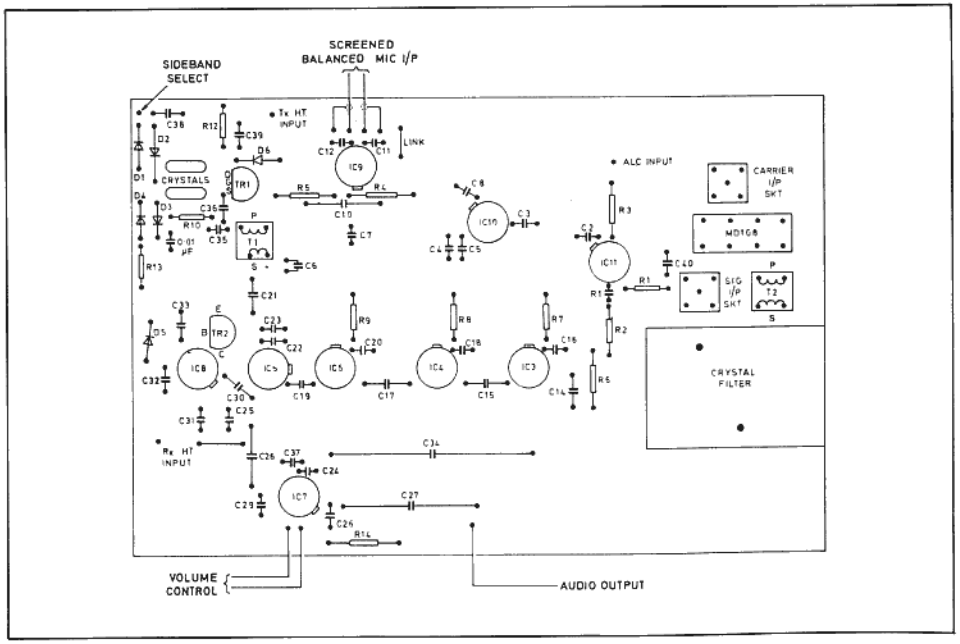

Fig.4 Component positions

PLSB22

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MP100 SERIES
MOS LOGIC ELEMENTS

Appendix C
A HIGH-PERFORMANCE ELECTRONIC MORSE KEYER

Early electronic morse keyers ensured that dots and dashes sent with a paddle key or squeeze key had the correct dot/dash ratio and weighting (mark/space ratio). In addition to possessing these features the system described in this application note incorporates a dot store (so that if the dot contact is briefly closed while a dash is being sent, then a dot will be sent automatically at the end of the dash before another dash can be sent) and will operate in the iambic mode. In this mode (which is alleged by its advocates to permit very high speeds), alternate dots and dashes are sent when both sides of a squeeze key are held together.

The logic for the keyer, shown in Fig. 1, consists of ten Plessey Semiconductors MP100 series MOS logic elements. Five MP106 type D flip-flops are connected as a shift register; the data input to bit 1 is permanently connected to logic '0' (+24V) so that as the register is clocked zeroes are propagated along it.

REST STATE

In the rest state, bits 1 – 4 of the shift register contain logic '0' the state of bit 5 being irrelevant. Gate 1 has logic '0' on all three inputs: $\overline{\text{RUN}}$ is false ('1') therefore, which inhibits the UJT timing oscillator (Fig. 2) and provides an enabling condition to gates 7 and 8. The dot store flip-flop is, however, in the reset state (pin 6 = logic '0'), disabling gate 8, while gate 7 is not enabled until a dash input occurs.

DASH INPUT

If a logic '1' is applied to the dash input, gate 7 is enabled and its logic '0' output sets shift register bits 1 and 2 directly, and bit 3 indirectly through gates 5 and 6, to logic '1'. The output of bit 3 turns on the output stage (Fig. 3) and enables gate 1: $\overline{\text{RUN}}$ is now true (logic '0'), the

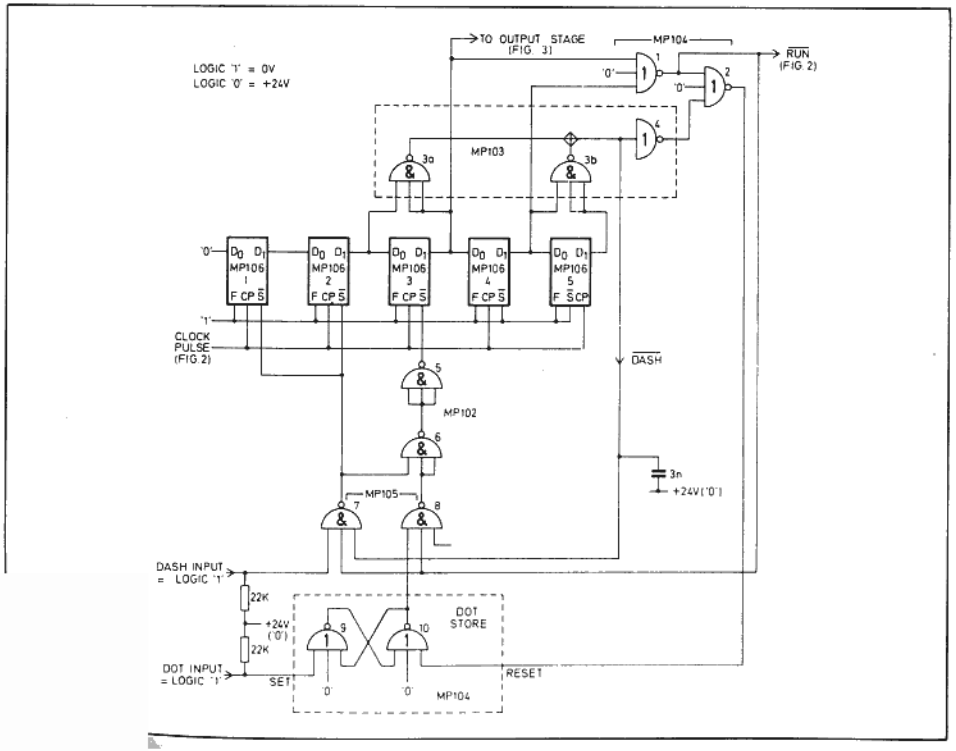

Fig. 1 Keyer logic

UJT oscillator is enabled and gates 7 and 8 are disabled to prevent further data from entering the system. At this point gate 3a recognises two logic '1' levels (indicating a dash in the system) and the output of gate 2 (which in the rest state was held at logic '0' by the input from gate 1) is maintained at logic '0' by the logic '1' from gate 4.

The UJT oscillator now runs for four pulses. After the second pulse, which shifts logic '1' into bit 5, gate 3b is enabled and takes over the function of keeping gate 3 output at logic '0'. After the fourth pulse the system re-enters the rest state. If no further signal is present on the inputs to either gate 7 or gate 8, the rest state persists and the oscillator remains off. The keyer has thus generated a single dash, consisting of a mark three timing spaces long followed by a space which is one timing space long.

If, on the other hand, there is a new dot or dash input, or there has been a dot input during the dash cycle, the keyer will continue to run. A dash input only, with no dot input having occurred, will cause the dash cycle to be repeated. A dot input will cause other events to occur.

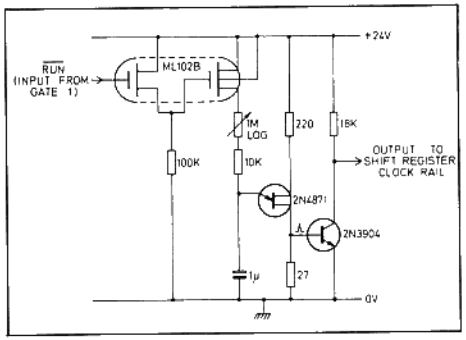

Fig. 2 Timing oscillator

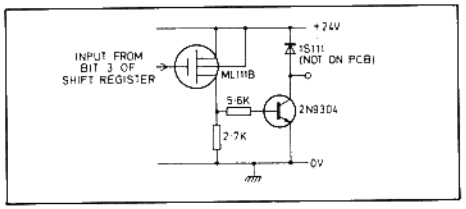

Fig. 3 Output stage

DOT INPUT

The dot input signal is connected to the set input of an R-S flip-flop which constitutes the dot store. If there is already a dot in the system (recognised at gate 2 by the combination of logic '0' outputs of gates 1 and 4) a logic '1' will be present on the flip-flop's reset input and the flip-flop will not set, both outputs being logic '0'. Conversely, if there is no logic '1' on the reset input (as is the case either when the system is at rest or during a dash cycle) a dot is stored in the flip-flop and gate 10 output is logic '1'. This, as soon as gate 1 output goes to logic '1' at the end of a cycle, enables gate 8. The resulting logic '0' at gate 5 output sets bit 3 of the shift register to logic '1', which in turn enables the system output and, after inversion via gate 1, turns on the timing oscillator. All three inputs to gate 2 are now logic '0' so that the resulting logic '1' output resets the dot store flip-flop.

Only two clock pulses are now required for the system to reach the rest state. On the first pulse the '1' in bit 3 is shifted into bit 4 and a '0' is shifted into bit 3 from bit 2: bit 3 output turns off the system output while the '1' now in bit 4 allows the oscillator to continue. The second pulse shifts the '1' out of bit 4 into bit 5 and a '0' into bit 4, disenabling the oscillator. Thus a dot has been generated, i.e. a mark one timing space long followed by a space of one timing space.

If both dot and dash inputs are present when bits 1 to 4 of the shift register have been zeroed then the next state of the register will depend on its previous contents. As soon as the register reaches the rest state the oscillator stops, gate 1 output goes to logic '1' and gate 2 to logic '0'. Gates 7 and 8 are 'primed', therefore, and the logic '0' from gate 2 allows the dot input to set the dot store flip-flop. However, the capacitor on the output of gate 3 ensures that there is a delay of several tens of microseconds after the end of a dash before the output of gate 3 can fall to logic '1', and hence before gate 7 can be enabled. Long before this can happen a dot will have entered the system, the oscillator will be running and gate 2 inhibited by the output of gate 1. If gate 3 has a logic '1' output before the rest state, the delay will be ineffective and a dash may enter the system.

Hence, if the system is presented with both dot and dash inputs then a dot will be generated if a dash was the previous state, and a dash will be generated if the system contained a dot or was at rest. Thus, the system will cause alternate dots and dashes to be sent, permitting operation in the iambic mode.

PERFORMANCE

The keyer consumes less than 25mA at a supply of 24V, and is capable of sending rates from 2 to 200 words per minute with the stated values of oscillator timing components. In the prototype, a 2N4871 unijunction transistor and two 2N3904 silicon NPN transistors were used; in fact, almost any UJT could be used, and any silicon NPN transistor with $V_{CEO} \geqslant 30V$ and $I_C(max) \geqslant 200mA$ will perform well.

CONSTRUCTION

The printed circuit board measures only 3.75 cm x 11.5 cm and is shown in Figs. 4 and 5. Although the integrated circuit count seems high it should be noted that the MP100 family contains only simple, inexpensive circuits – generally used for system breadboarding. The board is close-packed and not all interconnections are printed; seven wired links must be made. These are:–

1. Output gate 3 (pin 1) to input gate 7 (pin 7)
2. Output shift register bit 2 (pin 8) to input gate 3a (pin 8)
3. Dash input (DA) to input gate 7 (pin 6)
4. Dot input (DI) to input gate 9 (pin 8)
5. Output shift register bit 3 (pin 8) to gate of ML111B (pin 2) in output circuit.
6. Output gate 5 (pin 9) to $\overline{S}$ input of shift register bit 3 (pin 6)
7. Output gate 1 (pin 4) to pin 2 of ML102B.

PARTS LIST

Plessey Semiconductors

MP102B –	2 off
MP103B –	1 off
MP104B –	2 off
MP106B –	5 off
ML102B –	1 off
ML111B –	1 off

Resistors (all 1/8W)

27Ω –	1 off
220Ω –	1 off
2.7kΩ –	1 off
5.6kΩ –	1 off
10kΩ –	1 off
18kΩ –	1 off
22kΩ –	2 off
100kΩ –	1 off

Capacitors

1μF, 35V, Tantalum
0.003μF Wee Con

Transistors and Diodes

2N4871	1 off
2N3904	2 off
1S111	1 off

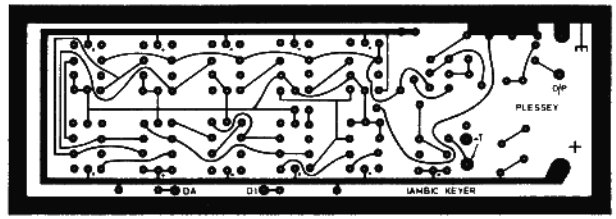

Fig. 4 PCB copper side

SCALE $\sqrt{2}:1$

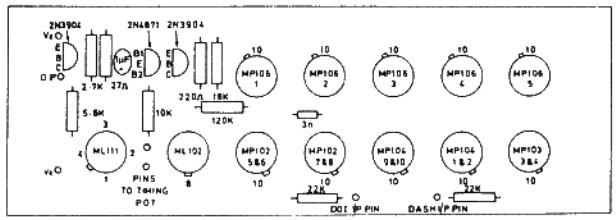

Fig. 5 Component locations

Appendix D

MULTIMODE TRANSCEIVER

This unit forms the heart of an AM, FM, CW and SSB transceiver for use in the frequency range 10 kHz to 500 MHz. The unit is constructed on a single printed circuit board and requires only a local oscillator, linear amplifier, pre-selector, microphone and audio amplifier to complete the transceiver. A block diagram is given in Fig. 1; detailed circuit diagrams are given in Fig. 2 (receiver section) and Fig. 3 (transmitter section).

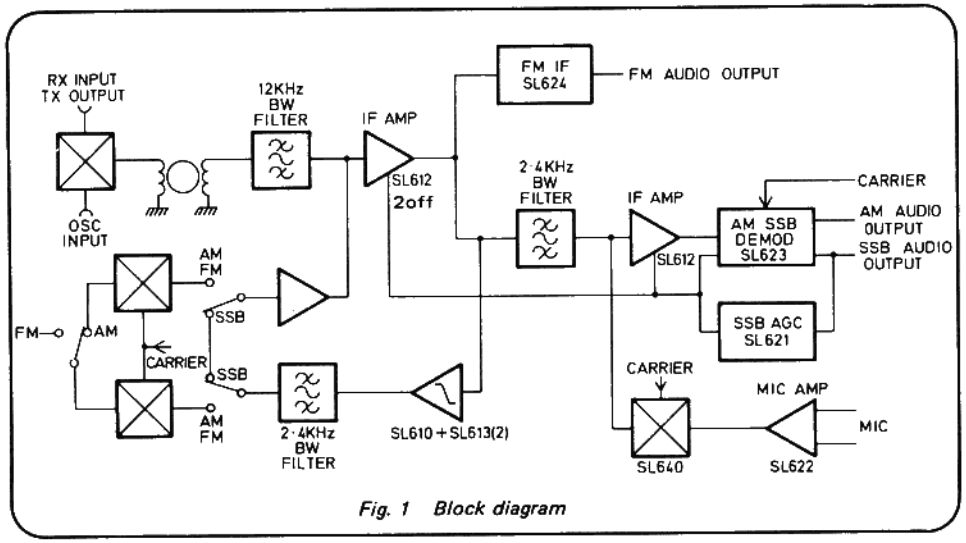

Fig. 1 Block diagram

RECEIVER

The receiver is a single conversion superhet with a 9 MHz intermediate frequency. The input mixer is an ANZAC MD108 diode ring mixer with a transmission line transformer on the output to match to the following crystal filter. The first crystal filter is 12 kHz wide to define the FM bandwidth, and is followed by two SL612C IF amplifiers. At this point the signal paths are split: the FM passing to an SL624C limiting amplifier/FM Detector and the AM/SSB/CW to a 2.4 KHz wide crystal filter. The AM/SSB is further amplified by another SL612C and demodulated by an SL623C. AGC is provided by the SL623C on AM and FM and by an SL621C on CW/SSB. On SSB the SL621C provides the AGC as it is more sensitive than the SL623C AGC. On AM, the carrier oscillator is switched off and hence, with no output from the product detector to operate the SL621C, the SL623C AGC takes over control. The board has three audio outputs: FM, AM and CW/SSB, which have to be switched externally into an audio amplifier.

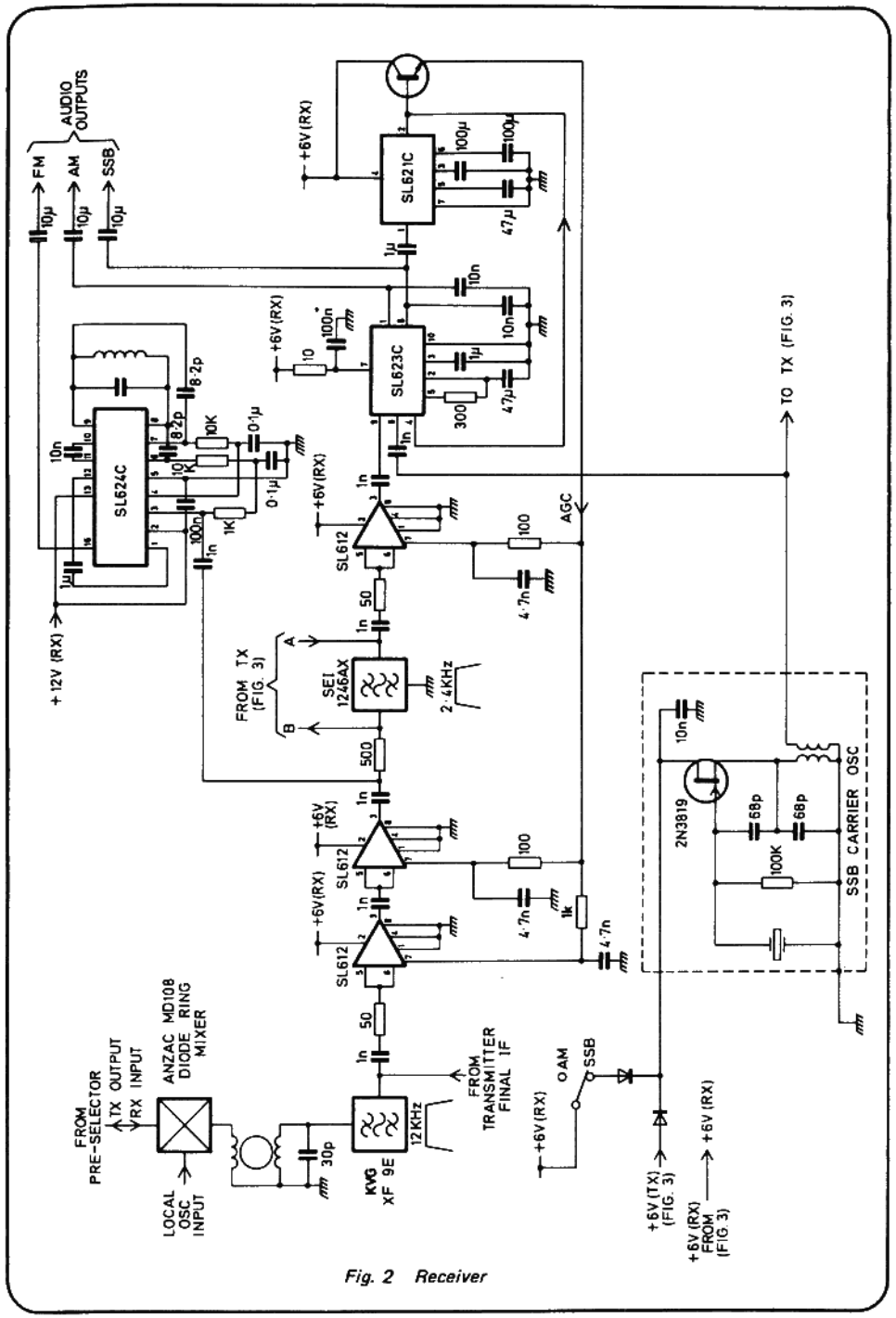

Fig. 2 Receiver

TRANSMITTER

An SL622C is used as the microphone pre-amplifier. This device has its own AGC, which automatically adjusts the output to suit the SL640C balanced modulator. The receiver 2.4 kHz wide crystal filter is used for sideband selection and is followed by an SL610C and two SL613C limiting amplifiers to obtain 20 db at RF clipping. A further 2.4 kHz wide filter is used to remove the unwanted products of the clipping process. On SSB RLA and RLC are energised; the signal is switched straight to an SL610C final IF amplifier, and applied through the 12 kHz filter to the mixer. For AM and FM the compressed SSB is demodulated by an SL640C to give a compressed audio frequency signal. Relays RLB and RLD are energised for FM; the audio signal is then switched via RLB/1 to the VFO. The opening of RLD/1 removes the AGC voltage applied to pin 7 of the SL610: the gain of the final IF amplifier is thus increased on FM to give full power output from the unmodulated carrier from the second SL640. On AM the compressed audio amplitude modulates the second SL640.

On CW the Transmitter mode is set to FM and a 10 KΩ resistor is connected from one side of the microphone input to earth. The CW signal is generated by keying the changeover from Receive to Transmit. The two stabilisers on the HT rails produce low impedance supplies with fast switching characteristics. For this form of keying the remaining parts of the transceiver, i.e. antenna relay and linear amplifier, have to be able to switch at the required rate. If this is not possible it is suggested that conventional keying of an AF oscillator is used.

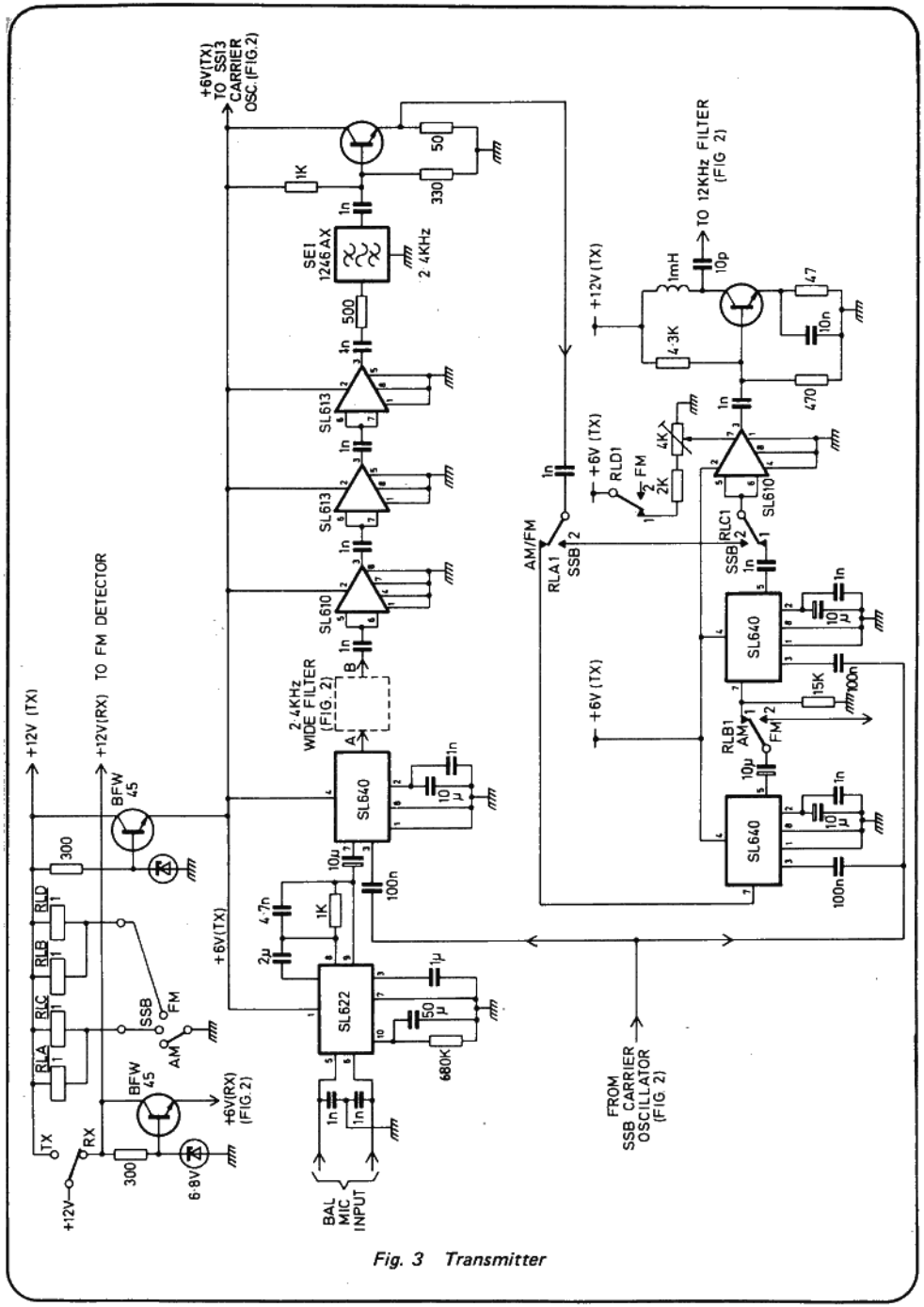

Fig. 3 Transmitter